SPECIFICATION

LIQUID CRYSTAL DISPLAY MODULE

Model No. **UMNH-7244JN-1F**

☐ **CUSTOMER :** _____

TENTATIVE

APPROVED SIGNATURE			
VERSION NO. 0			

SAMPLE 0

U.R.T. UNITED RADIANT TECHNOLOGY CORP.

APPROVED BY: _____ **DATE:** _____

LCM FACTORY: No12,Chien Kuo Road, Taichung Export Processing Zone ,Tantzu,Taichung,Taiwan,R.O.C
TEL:886-4-25314277 FAX:886-4-25340575
SALES OFFICE: 2F,No.19,Lane 768,Pa Teh Road Sec.4,Taipei ,Taiwan,R.O.C
TEL:886-2-27850792 FAX:886-2-27850797

CONTENTS:

Revision record

Module number	Rev mark	Revision description	Rev by	Rev date	Sample No.
UMNH-7244JN-F	0	1. Without LCD SPEC.	廖 志 豪 USNH-E533JY-F	Oct/4/01’	0
UMNH-7244JN-1F	0	1. Without LCD SPEC. 2. Changed the Vop of LCD from 13.0V to 15.5 V.	廖 志 豪 USNH-E533JY-1F	Oct/4/01’	0

1. Basic Specifications

1-1 Mechanical specifications:

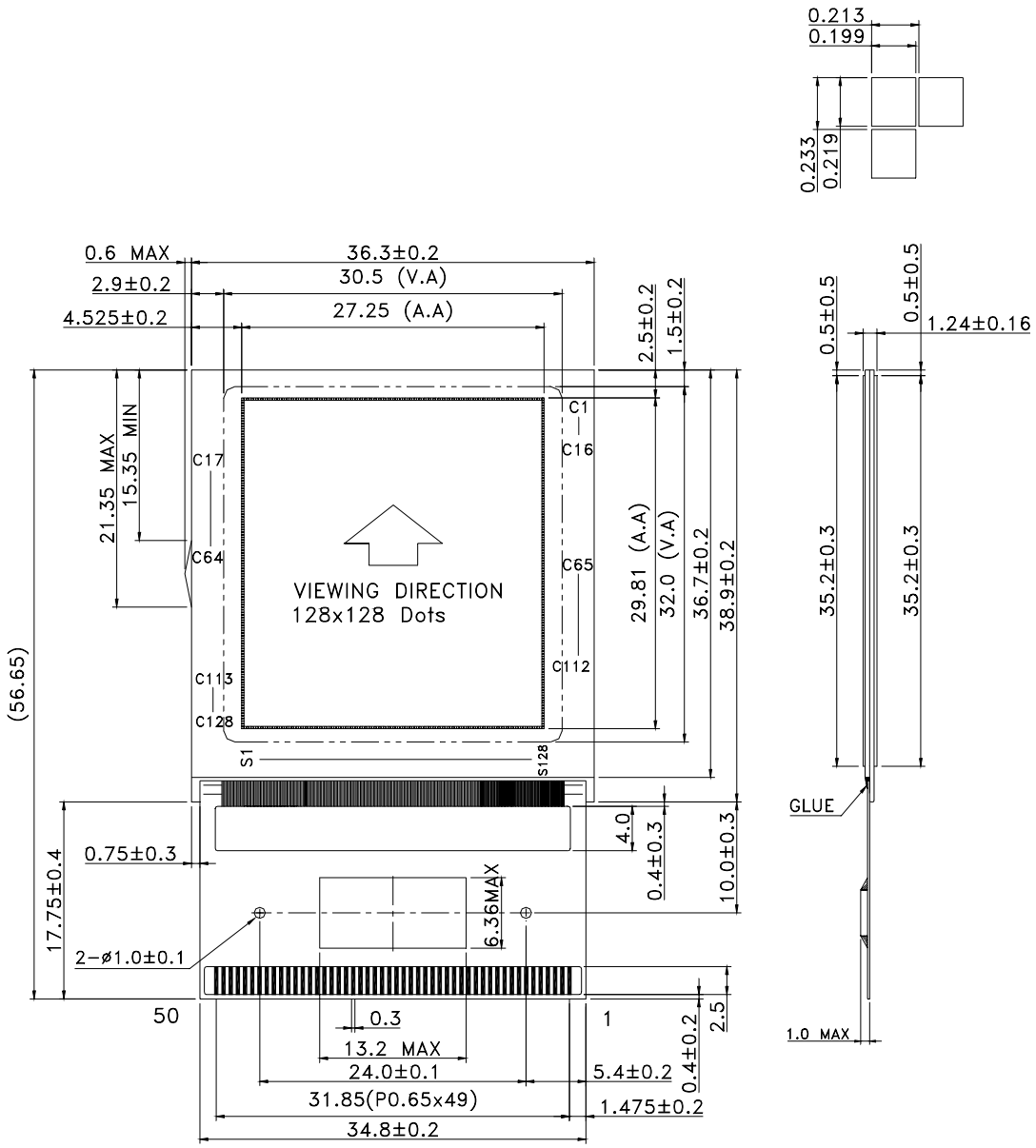
Items	Nominal Dimension	Unit
Dot Matrix	128 X128 dots	—
Module Size (W X H X T)	36.9 X 56.65 X 1.24	mm.
Viewing Area (W X H)	30.5 X 32.0	mm.
Active Area (W X H)	27.25 X 29.81	mm.
Dot Size (W X H)	0.199 X 0.219	dots
Dot Pitch (W X H)	0.213 X 0.233	mm.
Driving Method	1/128	Duty
	1/11	Bias
Driving IC Assembly	TAB	—

＊ Exporse the driver IC under blaze (luminosity over than 1 cd) when using the LCM may cause IC operating failure.

1-2 Display Specifications:

Display	Descriptions	Note
LCD Type	FSTN	
LCD Mode	Positive	
Polarizer Mode	Transflective	
Polarizer UV - Cutting	With	
Polarizer Surface	Normal	
Background Color	White	
Backlight Type	-	
Backlight Color	-	
Viewing Angle	12 O‘clock Direction	

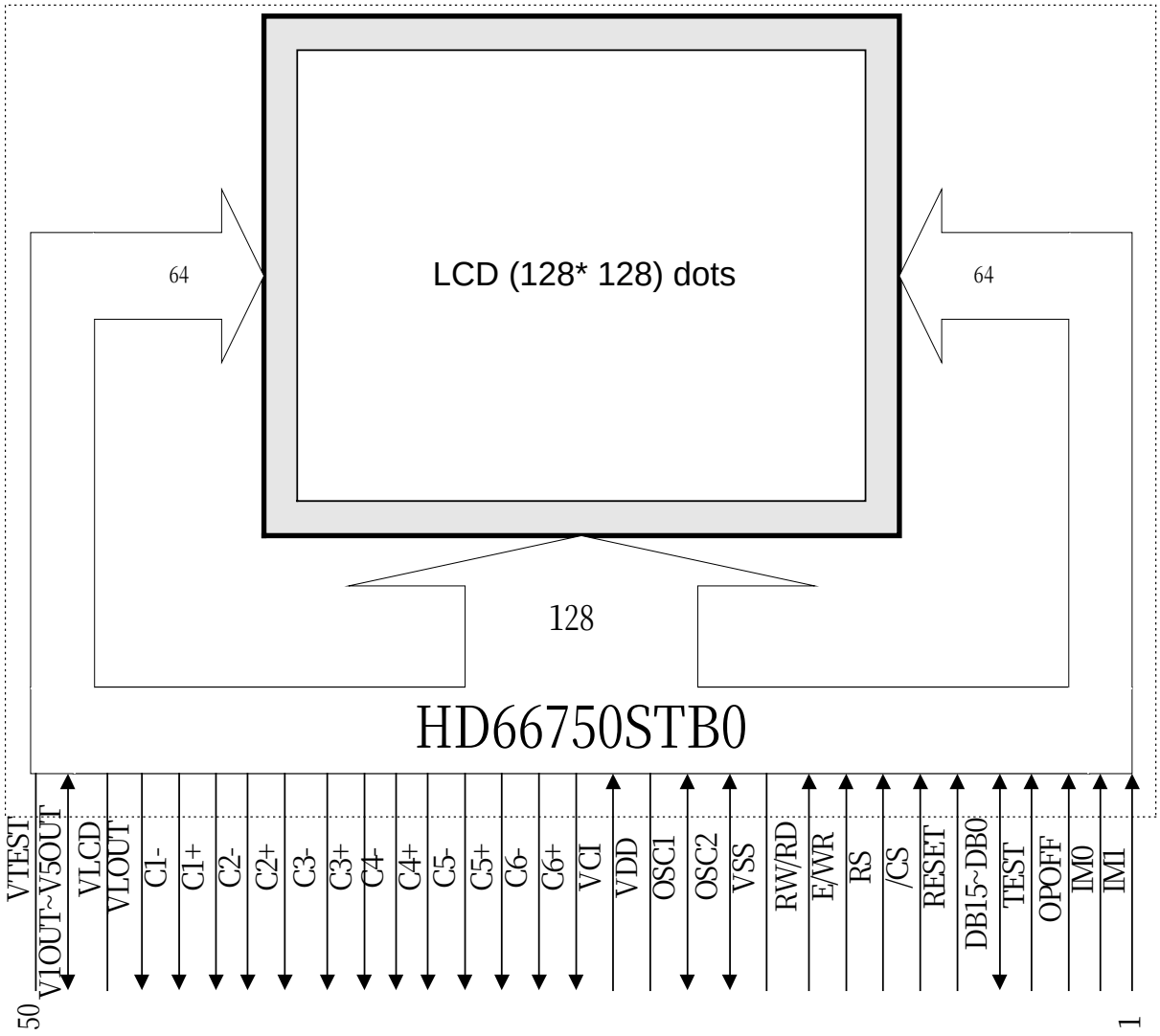
1-3 Outline Dimension



NOTE:

1. DRIVER IC : HD66750STB0
2. LCD FSTN TYPE, TRANSFLECTIVE
3. VIEWING DIRECTION 6 O'CLOCK, 128x128 DOTS
4. Top : −20 ~ 70 °C, Tst : −30 ~ 80 °C

1-4 Block Diagram



1-5 Interface Pin Connection:

Pin No.	Pin Name	I/O	Description
1	IM1	I	Selects the MPU interface mode: IM1 IM0 MPU interface mode GND GND 68-system 16-bit bus interface GND VCC 68-system 8-bit bus interface VCC GND 80-system 16-bit bus interface VCC VCC 80-system 8-bir bus interface
2	IM0		
3	OPOFF	I	Turns the internal operational amplifier off when OPOFF=VCC, and turns it on when OPOFF=GND. If the amplifier is turned off (OPOFF=VCC), V1 to V5 must be supplied to the V1OUT to V5OUT pins.
4	TEST	I	Test pin. Must be fixed at GND level.
5~20	DB15~DB0	I/O	Serves as a 16-bit bi-directional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the Vcc or GND level.
21	RESET	I	Reset pin. Initializes the LSI when low. Must be reset after power-on.
22	/CS	I	Selects the HD66750STB0： Low： HD66750STB0 is selected and can be accessed. High： HD66750STB0 is not selected and cannot be accessed. Must be fixed at GND level when not in use.
23	RS	I	Selects the register. Low： Index/status High：Control
24	E/WR	I	For a 68-system bus interface, serves as an enable signal to activate data read/write operation. For an 80-system bus interface, serves as a write strobe signal and writes data at the low level.

Pin No.	Pin Name	I/O	Description
25	RW/RD	I	For a 68-system bus interface, serves as a signal to select data read/write operation. Low: Write High: Read For an 80-system bus interface, serves as a read strobe signal and reads data at the low level.
26	VSS	-	Ground.
27,28	OSC2,OSC 1	I/O	For R-C oscillation using an external resistor, connect an external resistor. For external clock supply, input clock pulses to OSC1.
29	VDD	-	Power supply. (+3.0V)
30	VCI	-	Inputs a reference voltage and supplies power to the booster; generates the liquid crystal display drive voltage from the operating voltage. The boosting output voltage must not be larger than the absolute maximum ratings. Must be left disconnected when the booster is not used
31,32	C6+ ,C6-	-	External capacitance should be connected here for boosting
33,34	C5+ ,C5-	-	External capacitance should be connected here for boosting
35,36	C4+ ,C4-	-	External capacitance should be connected here for boosting
37,38	C3+ ,C3-	-	External capacitance should be connected here for boosting
39,40	C2+ ,C2-	-	External capacitance should be connected here for boosting
41,42	C1+ ,C1-	-	External capacitance should be connected here for boosting
43	VLOUT	O	Potential difference between Vci and GND is two- to seven-times-boosted and then output. Magnitude of boost is selected by instruction
44	VLCD	-	Power supply for LCD drive. VLCD-GND = 17V max.
45~49	V1OUT~ V5OUT	I/O	Used for output from the internal operational amplifiers when they are used (OPOFF = GND); attach a capacitor to stabilize the output. When the amplifiers are not used (OPOFF = VCC), V1 to V5 voltages can be supplied to these pins externally.
50	VTEST		Test pin. Must be left disconnected.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

(vss = 0V)

Items	Symbol	Min.	Max.	Unit
Supply voltage for logics	VDD-VSS	-0.3	+4.6	V
Supply voltage for driving LCD	V_{LOUT}-VSS	-0.3	+16.5	V
Input voltage	V_{IN}	-0.3	VDD+0.3	V
Operating temperature range	T_{OP}	-20	70	℃
Storage temperature range	T_{ST}	-30	80	℃

2.2 DC Characteristics

(VDD=3.0±0.5V,VSS=0V, T_a=25°C)

Items	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply voltage (Logic)	V_{DD}	-	3.0	-	V	
Supply voltage (LCD)	V_{op}	-	15.5	-	V	*NOTE1
Input high level voltage	V_{IH}	0.7VDD	-	VDD	V	
Input low level voltage	V_{IL}	-0.3	-	0.15VDD	V	
Output high level voltage	V_{OH}	0.75VDD	-	-	V	
Output low level voltage	V_{OL}	-	-	0.15VDD	V	
Power supply current (VDD)	I_{DD}	-	-	2.0	mA	*NOTE2

*NOTE1 : Min. and Max. Voltage is specified as the voltage within the condition of operational temperature range -20°C ~ 70°C.

Typ. Voltage is specified as module driving condition: T_a=25°C.

V_{op} (=V1-GND)

Vop set instruction description

	Code															
	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Contrast control	*	*	*	*	*	*	*	*	*	*	1	0	1	0	0	1

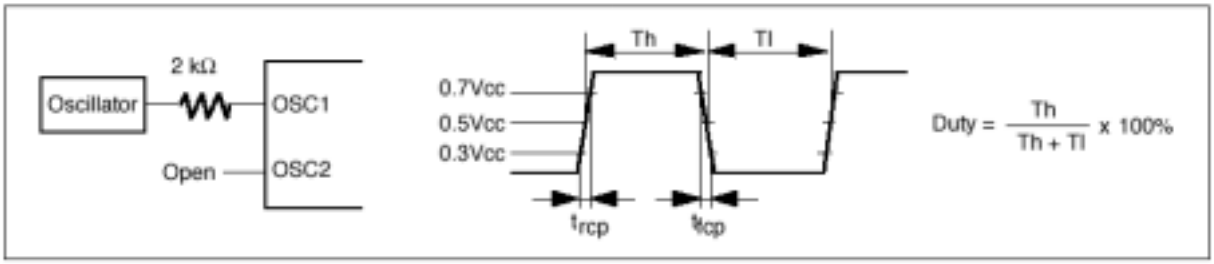
*NOTE2 :
Measuring Condition:
Standard Value MAX.

T_a	= 25°C
VDD-VSS	= 3.0V
VCI-VSS	= 3.0V
V_{1OUT}-VSS	= V_{OP} at optimum contrast
Duty	= 1/128 Duty
Bias	= 1/11Bias
Display Pattern	= Checkered pattern

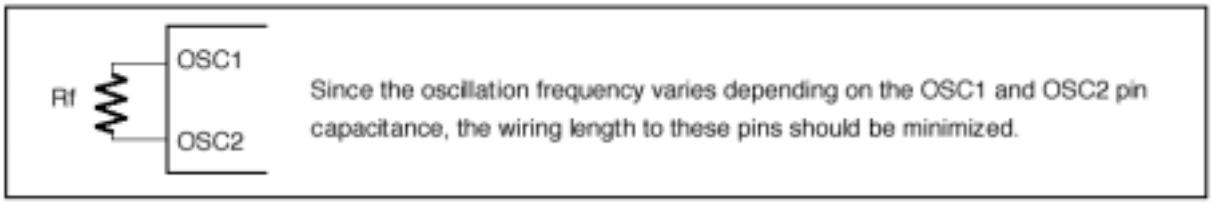
2.3 AC Characteristic

Clock Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition
External clock frequency	fcp	50	75	150	kHz	
External clock duty ratio	Duty	45	50	55	%	
External clock rise time	trcp	—	—	0.2	µs	
External clock fall time	tfcp	—	—	0.2	µs	
R-C oscillation clock	f_{osc}	59	74	89	kHz	Rf = 390 kΩ, V_{CC} = 3 V



External Clock Supply



Internal Oscillation

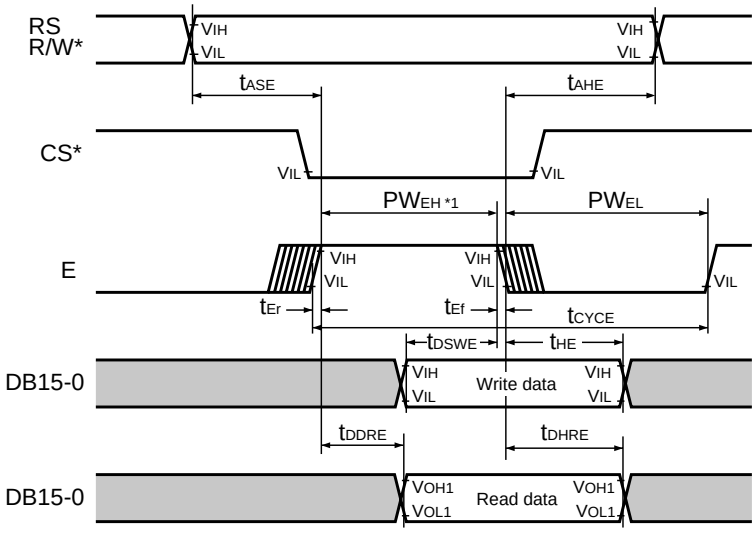
External	R-C Oscillation Frequency: fosc			
Resistance (Rf)	Vcc = 1.8 V	Vcc = 2.2 V	Vcc = 3.0 V	Vcc = 4.0 V
200 kΩ	86 kHz	111 kHz	130 kHz	140 kHz
270 kΩ	70 kHz	86 kHz	100 kHz	108 kHz
300 kΩ	64 kHz	79 kHz	92 kHz	98 kHz
330 kΩ	60 kHz	74 kHz	86 kHz	91 kHz
360 kΩ	57 kHz	69 kHz	79 kHz	84 kHz
390 kΩ	54 kHz	64 kHz	74 kHz	78 kHz
430 kΩ	49 kHz	59 kHz	67 kHz	71 kHz
470 kΩ	46 kHz	54 kHz	61 kHz	65 kHz

External Resistance Value and R-C Oscillation Frequency (Referential Data)

(VDD=3.0V)

68-system Interface Timing Characteristics

Item		Symbol	Min	Typ	Max	Unit
Enable cycle time	Write	t_{CYCE}	380	—	—	ns
	Read	t_{CYCE}	500	—	—	
Enable high-level pulse width	Write	PW_{EH}	70	—	—	ns
	Read	PW_{EH}	250	—	—	
Enable low-level pulse width	Write	PW_{EL}	150	—	—	ns
	Read	PW_{EL}	150	—	—	
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns
Setup time (RS, R/W to E, CS*)		t_{ASE}	50	—	—	ns
Address hold time		t_{AHE}	20	—	—	ns
Write data setup time		t_{DSWE}	60	—	—	ns
Write data hold time		t_{HE}	20	—	—	ns
Read data delay time		t_{DDRE}	—	—	200	ns
Read data hold time		t_{DHRE}	5	—	—	ns



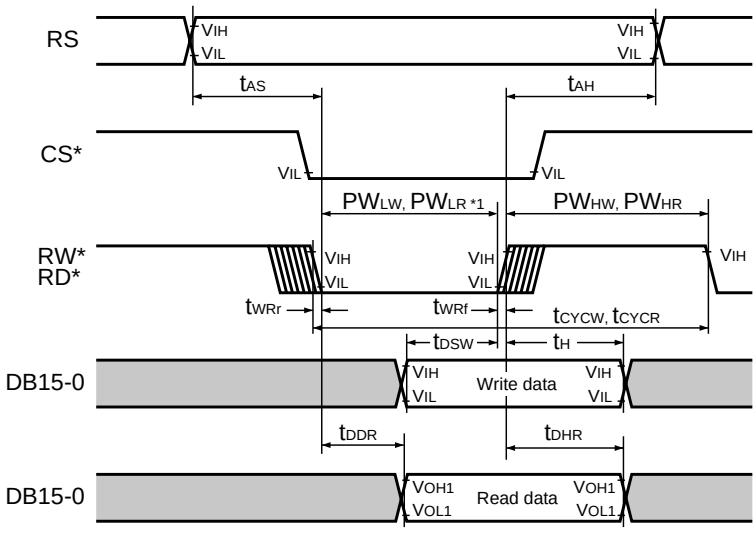
Note : PW_{EH} is specified in the overlapped period when CS* is low and E is high.

68-system Bus Timing

(VDD=3.0V)

80-system Bus Interface Timing Characteristics

Item		Symbol	Min	Typ	Max	Unit
Bus cycle time	Write	t_{CYCW}	380	—	—	ns
	Read	t_{CYCR}	500	—	—	ns
Write low-level pulse width		PW_{LW}	70	—	—	ns
Read low-level pulse width		PW_{LR}	250	—	—	ns
Write high-level pulse width		PW_{HW}	150	—	—	ns
Read high-level pulse width		PW_{HR}	150	—	—	ns
Write/Read rise/fall time		$t_{WRr, WRf}$	—	—	25	ns
Setup time (RS to CS*, WR*, RD*)		t_{AS}	50	—	—	ns
Address hold time		t_{AH}	20	—	—	ns
Write data setup time		t_{DSW}	60	—	—	ns
Write data hold time		t_H	20	—	—	ns
Read data delay time		t_{DDR}	—	—	200	ns
Read data hold time		t_{DHR}	5	—	—	ns

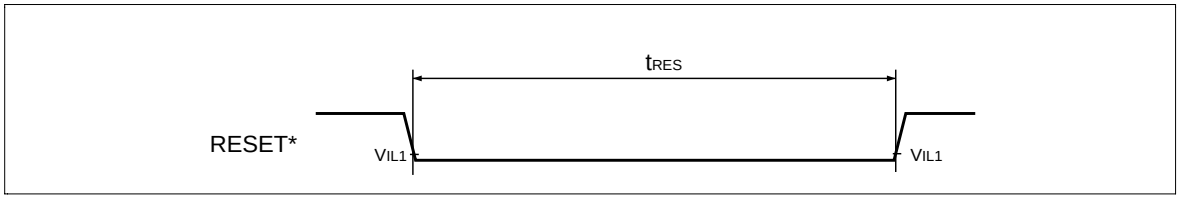


Note : PW_{LW} and PW_{LR} are specified in the overlapped period when CS* is low and WR* or RD* is low.

80-system Bus Timing

2-4 Reset Timing:

Item	Symbol	Min	Typ	Max	Unit
Reset low-level width	t_{RES}	1	—	—	ms



3. Optical Characteristics

3.1 Optical Characteristics

Driving Condition

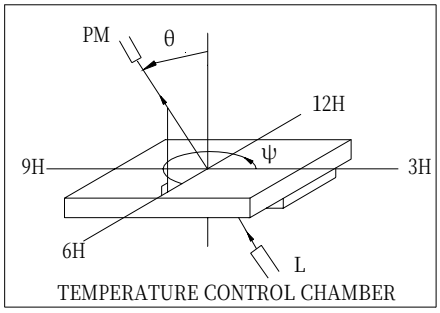
Item	Voltage	Duty	Bias
Valu	15.5V	1/128	1/11

Electrical/Optical Characteristics

No	Item		Symbol/Temp.		MIN.	TYP.	MAX.	Unit.	Remarks
1	Vth Voltage		-20℃	Vth2	-	-	-	V	Note2
				Vth1	-	-	-		
			25℃	Vth2	-	-	-		
				Vth1	-	-	-		
			70℃	Vth2	-	-	-		
				Vth1	-	-	-		
2	Response Time		Tf	-20℃	-	-	-	ms	Note4
				25℃	-	-	-		
				70℃	-	-	-		
			Tf	-20℃	-	-	-		
				25℃	-	-	-		
				70℃	-	-	-		
3	Viewing Angle	Front-Rear	Θ1	Φ=270	-	-	-	deg.	Note1
		Left-Right	Θ2		-	-	-		
4	Contrast Ratio		Cr	25℃	-	-	-	-	Note7

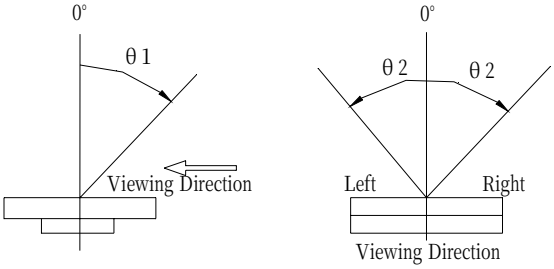
3.2 Definition of Optical Characteristics

Measurement Condition
L: LIGHT SOURCE
PM: LIGHT RECEIVING PHOTOMULTIPLIER TUBE

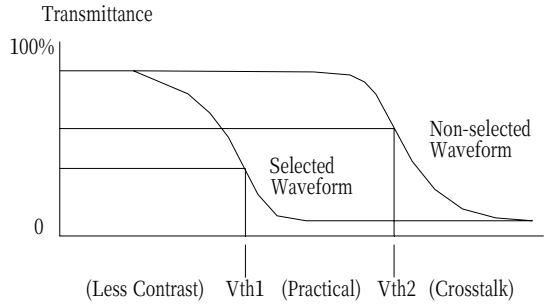


[Note 1] Definition of Viewing Angle

Viewing Direction: ψ=270°

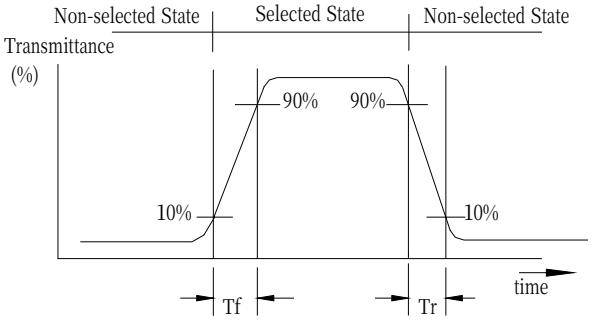


[Note 2] Definition of "Vth"



(a). Vth1: ψ=270°, θ 1=10°, Selected Waveform 50% Transmittance
(b). Vth1: ψ=270°, θ 1=40°, Non-selected Waveform 70% Transmittance

[Note 4] Definition of Response Time



Measurement Condition: Viewing Angle: θ 2=0°, θ 1=0°

[Note 3] Definition of Contrast Ratio

(a). Contrast Ratio= $\frac{\text{Transmittance under Non-selected Waveform}}{\text{Transmittance under Selected Waveform}}$

(b). Measurement Condition: Viewing Angle: θ 2=0° , θ 1=10°

4. Control And Display Command
4-1 Reset Function

Reset Function

The HD66750S is internally initialized by RESET input. Because the HD66750S is a busy state during the reset period, no instruction or CGRAM data access from the MPU is accepted. The reset input must be held for at least 1 ms. Do not access the CGRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (CN = 0, NL3–0 = 1111, SGS = 0, CMS = 0)
3. B-pattern waveform AC drive (B/C = 0, ECR = 0, NW4–0 = 00000)
4. Power control (DC1–0 = 00, AP1–0 = 00: LCD power off, SLP = 0: Sleep mode off, STB = 0: Standby mode off)
5. 1/11 bias drive (BS2–0 = 000), Two-times boost (BT1–0 = 00), Weak contrast (CT5–0 = 000000)
6. Entry mode set (I/D = 1: Increment by 1, AM1–0 = 00: Horizontal move, LG1–0 = 00: Replace mode)
7. Rotation (RT2–0 = 000: No shift)
8. Display control (DHE = 0: Double-height display off, REV = 0, GS = 0, D = 0: Display off, PS1–0 = 00: Partial scroll off)
9. Cursor control (C = 0: Cursor display off, CM1–0 = 00: White blink cursor)
10. Double-height display position (DS6–0 = 0000000, DE6–0 = 0000000)
11. Vertical scroll control (SL6–0 = 0000000: First raster-row displayed at the top)
12. Window cursor display position (HS6–0 = HE6–0 = VS6–0 = VE6–0 = 0000000)
13. RAM write data mask (WM15–0 = 0000H: No mask)
14. RAM address set (AD10–0 = 000H)

CGRAM Data Initialization:

This is not automatically initialized by reset input but must be initialized by software while display is off (D = 0).

Output Pin Initialization:

1. LCD driver output pins (SEG/COM): Outputs GND level
2. Booster output pins (VLOUT): Outputs Vcc level
3. Oscillator output pin (OSC2): Outputs oscillation signal

4.2 Inuctstrion Table

Reg. No.	Register Name	R/W	RS	Upper Code DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	Lower Code DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle
IR	Index	0	0	-	-	-	-	-	-	-	-	-	-	-	ID4	ID3	ID2	ID1	ID0	Sets the index register value.	0
SR	Status read	1	0	0	L6	L5	L4	L3	L2	L1	L0	0	0	C5	C4	C3	C2	C1	C0	Reads the dirming reader-row position (L6–0) and contrast setting (C5–0).	0
R00	Start oscillation	0	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	Starts the oscillation mode.	10 ms
	Device code read	1	1	0	0	0	0	0	1	1	1	0	1	0	1	0	0	0	0	Reads 0750H.	0
R01	Driver output control	0	1	-	-	-	-	-	-	CMS	SGS	-	CN	-	-	NL3	NL2	NL1	NL0	Sets the common driver shift direction (CMS), segment driver shift direction (SGS), driving duty ratio (NL3–0), and centering (CN).	0
R02	LCD-driving-waveform control	0	1	-	-	-	-	-	-	-	-	-	BIC	EOR	NW4	NW3	NW2	NW1	NW0	Sets the LCD drive AC waveform (BIC), and EOR output (EOR) or the number of n-raster-rows (NW4–0) at C-pattern AC drive.	0
R03	Power control	0	1	-	-	-	BS2	BS1	BS0	BT1	BT0	-	-	DC1	DC0	AP1	AP0	SLP	STB	Sets the sleep mode (SLP), standby mode (STB), LCD power on (AP1–0), boosting cycle (DC1–0), boosting ouput multiplying factor (BT1–0), and LCD drive bias value (BS2–0).	0
R04	Contrast control	0	1	-	-	-	-	-	-	-	-	-	-	CT5	CT4	CT3	CT2	CT1	CT0	Sets the contrast adjustment (CT5–0).	0
R05	Entry mode	0	1	-	-	-	-	-	-	-	-	-	-	-	I/D	AM1	AM0	LG1	LG0	Specifies the logical operation (LG1–0), AC counter mode (AM1–0), and increment/decrement mode (I/D).	0
R06	Relation	0	1	-	-	-	-	-	-	-	-	-	-	-	-	-	RT2	RT1	RT0	Specifies the amount of write-data rotation (RT2–0).	0
R07	Display control	0	1	-	-	-	-	-	-	-	-	-	-	PS1	PS0	DHE	GS	REV	D	Specifies display on (D), black-and-white reversed display (REV), grayscale mode (GS), double-height display on (DHE), and partial scroll (PS1–0).	0
R08	Cursor control	0	1	-	-	-	-	-	-	-	-	-	-	-	-	-	C	CM1	CM0	Specifies cursor display on (C) and cursor display mode (CM1–0).	
R09	Double-height display position	0	1	-	DE6	DE5	DE4	DE3	DE2	DE1	DE0	-	DS6	DS5	DS4	DS3	DS2	DS1	DS0	Specifies double-height display start (DS6–0) and end (DE6–0).	0
R0A	Vertical scroll	0	1	-	-	-	-	-	-	-	-	-	SL6	SL5	SL4	SL3	SL2	SL1	SL0	Sets the display-start raster-row (SL6–0).	0
R0B	Horizontal cursor position	0	1	-	HE6	HE5	HE4	HE3	HE2	HE1	HE0	-	HS6	HS5	HS4	HS3	HS2	HS1	HS0	Sets horizontal cursor start (HS6–0) and end (HE6–0).	0
R0C	Vertical cursor position	0	1	-	VE6	VE5	VE4	VE3	VE2	VE1	VE0	-	VS6	VS5	VS4	VS3	VS2	VS1	VS0	Sets vertical cursor start (VS6–0) and end (VE6–0).	0
R10	RAM write data mask	0	1	WM 15	WM 14	WM 13	WM 12	WM 11	WM 10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	Specifies write data mask (WM15–0) at RAM write.	0
R11	RAM address set	0	1	-	-	AD10–8 (upper)						AD7–0 (lower)								Initially sets the RAM address to the address counter (AC).	0
R12	RAM data write	0	1	Write data (upper)								Write data (lower)								Writes data to the RAM.	0
	RAM data read	1	1	Read data (upper)								Read data (lower)								Reads data from the RAM.	0

Note: "-" means "doesn't matter".

Index

The index instruction specifies the RAM control indexes (R00 to R12). It sets the register number in the range of 00000 to 10010 in binary form.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	*	*	*	*	*	*	*	*	*	*	*	**ID4**	**ID3**	**ID2**	**ID1**	**ID0**

Index Instruction

Status Read

The status read instruction reads the internal status of the HD66750S.

L6–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

C5–0: Read the contrast setting values (CT5–0).

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	**0**	**L6**	**L5**	**L4**	**L3**	**L2**	**L1**	**L0**	**0**	**0**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**

Status Read Instruction

Start Oscillation

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

If this register is read forcibly when R/W = 1, 0750H is read.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	**1**
1	1	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**

Start Oscillation Instruction

Driver Output Control

CMS: Selects the output shift direction of a common driver. When CMS = 0, COM1/128 shifts to COM1, and COM128/1 to COM128. When CMS = 1, COM1/128 shifts to COM128, and COM128/1 to COM1. Output position of a common driver shifts depending on the CN bit setting.

SGS: Selects the output shift direction of a segment driver. When SGS = 0, SEG1/128 shifts to SEG1, and SEG128/1 to SEG128. When SGS = 1, SEG1/128 shifts to SEG128, and SEG128/1 to SEG1.

CN: When CN = 1, the display position is shifted down by 32 raster-rows and display starts from COM33. When the liquid crystal is driven at a low duty ratio in the system wait state, it can be partially displayed at the center of the screen. For details, see the Partial-display-on Function section.

NL3-0: Specify the LCD drive duty ratio. The duty ratio can be adjusted for every eight raster-rows. CGRAM address mapping does not depend on the setting value of the drive duty ratio.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	*	*	*	*	*	*	**CMS**	**SGS**	*	**CN**	*	*	**NL3**	**NL2**	**NL1**	**NL0**

Driver Output Control Instruction

NL Bits and Drive Duty

NL3	NL2	NL1	NL0	Display Size	LCD Drive Duty	Common Driver Used
0	0	0	0	128 x 8 dots	1/8 Duty	COM1–COM8
0	0	0	1	128 x 16 dots	1/16 Duty	COM1–COM16
0	0	1	0	128 x 24 dots	1/24 Duty	COM1–COM24
0	0	1	1	128 x 32 dots	1/32 Duty	COM1–COM32
0	1	0	0	128 x 40 dots	1/40 Duty	COM1–COM40
0	1	0	1	128 x 48 dots	1/48 Duty	COM1–COM48
0	1	1	0	128 x 56 dots	1/56 Duty	COM1–COM56
0	1	1	1	128 x 64 dots	1/64 Duty	COM1–COM64
1	0	0	0	128 x 72 dots	1/72 Duty	COM1–COM72
1	0	0	1	128 x 80 dots	1/80 Duty	COM1–COM80
1	0	1	0	128 x 88 dots	1/88 Duty	COM1–COM88
1	0	1	1	128 x 96 dots	1/96 Duty	COM1–COM96
1	1	0	0	128 x 104 dots	1/104 Duty	COM1–COM104
1	1	0	1	128 x 112 dots	1/112 Duty	COM1–COM112
1	1	1	0	128 x 120 dots	1/120 Duty	COM1–COM120
1	1	1	1	128 x 128 dots	1/128 Duty	COM1–COM128

LCD-Driving-Waveform Control

B/C: When B/C = 0, a B-pattern waveform is generated and alternates in every frame for LCD drive. When B/C = 1, a C-pattern waveform is generated and alternates in each raster-row specified by bits EOR and NW4–NW0 in the LCD-driving-waveform control register. For details, see the n-raster-row Reversed AC Drive section.

EOR: When the C-pattern waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the LCD drive duty ratio and the n raster-row. For details, see the n-raster-row Reversed AC Drive section.

NW4–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = 1). NW4–NW0 alternate for every set value + 1 raster-row, and the first to the 32nd raster-rows can be selected.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	*	*	*	*	*	*	*	*	*	**B/C**	**EOR**	**NW4**	**NW3**	**NW2**	**NW1**	**NW0**

LCD-Driving Waveform Control Instruction

Common Driver Pin Function

Common Driver Pin	Common Driver Pin Function			
	CN = 0 (Normal Output)		CN = 1 (Center Output)	
	CMS = 0	CMS = 1	CMS = 0	CMS = 1
COM1/128	**COM1**	COM128	COM97	COM96
⋮	⋮	⋮	⋮	⋮
COM8/121	COM8	COM121	COM104	COM89
COM9/120	COM9	COM120	COM105	COM88
⋮	⋮	⋮	⋮	⋮
COM16/113	COM16	COM113	COM112	COM81
COM17/112	COM17	COM112	COM113	COM80
⋮	⋮	⋮	⋮	⋮
COM24/105	COM24	COM105	COM120	COM73
COM25/104	COM25	COM104	(COM121)	COM72
⋮	⋮	⋮	⋮	⋮
COM32/97	COM32	COM97	(COM128)	COM65
COM33/96	COM33	COM96	**COM1**	COM64
⋮	⋮	⋮	⋮	⋮
COM40/89	COM40	COM89	COM8	COM57
COM41/88	COM41	COM88	COM9	COM56
⋮	⋮	⋮	⋮	⋮
COM48/81	COM48	COM81	COM16	COM49
COM49/80	COM49	COM80	COM17	COM48
⋮	⋮	⋮	⋮	⋮
COM56/73	COM56	COM73	COM24	COM41
COM57/72	COM57	COM72	COM25	COM40
⋮	⋮	⋮	⋮	⋮
COM64/65	COM64	COM65	COM32	COM33
COM65/64	COM65	COM64	COM33	COM32
⋮	⋮	⋮	⋮	⋮
COM72/57	COM72	COM57	COM40	COM25
COM73/56	COM73	COM56	COM41	COM24
⋮	⋮	⋮	⋮	⋮
COM80/49	COM80	COM49	COM48	COM17
COM81/48	COM81	COM48	COM49	COM16
⋮	⋮	⋮	⋮	⋮
COM88/41	COM88	COM41	COM56	COM9
COM89/40	COM89	COM40	COM57	COM8
⋮	⋮	⋮	⋮	⋮
COM96/33	COM96	COM33	COM64	**COM1**

Common Driver Pin Function (cont)

Common Driver Pin	Common Driver Pin Function			
	CN = 0 (Normal Output)		CN = 1 (Center Output)	
	CMS = 0	CMS = 1	CMS = 0	CMS = 1
COM97/32	COM97	COM32	COM65	(COM128)
⋮	⋮	⋮	⋮	⋮
COM104/25	COM104	COM25	COM72	(COM121)
COM105/24	COM105	COM24	COM73	COM120
⋮	⋮	⋮	⋮	⋮
COM112/17	COM112	COM17	COM80	COM113
COM113/16	COM113	COM16	COM81	COM112
⋮	⋮	⋮	⋮	⋮
COM120/9	COM120	COM9	COM88	COM105
COM121/8	COM121	COM8	COM89	COM104
⋮	⋮	⋮	⋮	⋮
COM128/1	COM128	**COM1**	COM96	COM97

Power Control

BS2–0: The LCD drive bias value is set within the range of a 1/4 to 1/11 bias. The LCD drive bias value can be selected according to its drive duty ratio and voltage. For details, see the Liquid Crystal Display Drive Bias Selector section.

BT1-0: The output factor of VLOUT between two-times, five-times, six-times, and seven-times boost is switched. The LCD drive voltage level can be selected according to its drive duty ratio and bias. Lower amplification of the booster consumes less current.

DC1-0: The operating frequency in the booster is selected. When the boosting operating frequency is high, the driving ability of the booster and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

AP1-0: The amount of fixed current from the fixed current source in the operational amplifier for V pins (V1 to V5) is adjusted. When the amount of fixed current is large, the driving ability of the booster and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption.

During no display, when AP1–0 = 00, the current consumption can be reduced by ending the operational amplifier and booster operation.

BS Bits and LCD Drive Bias Value

BS2	BS1	BS0	LCD Drive Bias Value
0	0	0	1/11 bias drive
0	0	1	1/10 bias drive
0	1	0	1/9 bias drive
0	1	1	1/8 bias drive
1	0	0	1/7 bias drive
1	0	1	1/6 bias drive
1	1	0	1/5 bias drive
1	1	1	1/4 bias drive

BT Bits and Output Level

BT1	BT0	V5OUT Output Level
0	0	Two-times boost
0	1	Five-times boost
1	0	Six-times boost
1	1	Seven-times boost

DC Bits and Operating Clock Frequency

DC1	DC0	Operating Clock Frequency in the Booster
0	0	32-divided clock
0	1	16-divided clock
1	0	8-divided clock
1	1	4-divided clock

AP Bits and Amount of Fixed Current

AP1	AP0	Amount of Fixed Current in the Operational Amplifier
0	0	Operational amplifier and booster do not operate.
0	1	Small
1	0	Middle
1	1	Large

SLP: When SLP = 1, the HD66750S enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. For details, see the Sleep Mode section. Only the following instructions can be executed during the sleep mode.

Power control (BS2–0, BT1–0, DC1–0, AP1–0, SLP, and STB bits)

During the sleep mode, the other CGRAM data and instructions cannot be updated although they are

retained.

STB: When STB = 1, the HD66750S enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section.

Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = 0)
b. Start oscillation
c. Power control (BS2–0, BT1–0, DC1–0, AP1–0, SLP, and STB bits)

During the standby mode, the CGRAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	*	*	*	**BS2**	**BS1**	**BS0**	**BT1**	**BT0**	*	*	**DC1**	**DC0**	**AP1**	**AP0**	**SLP**	**STB**

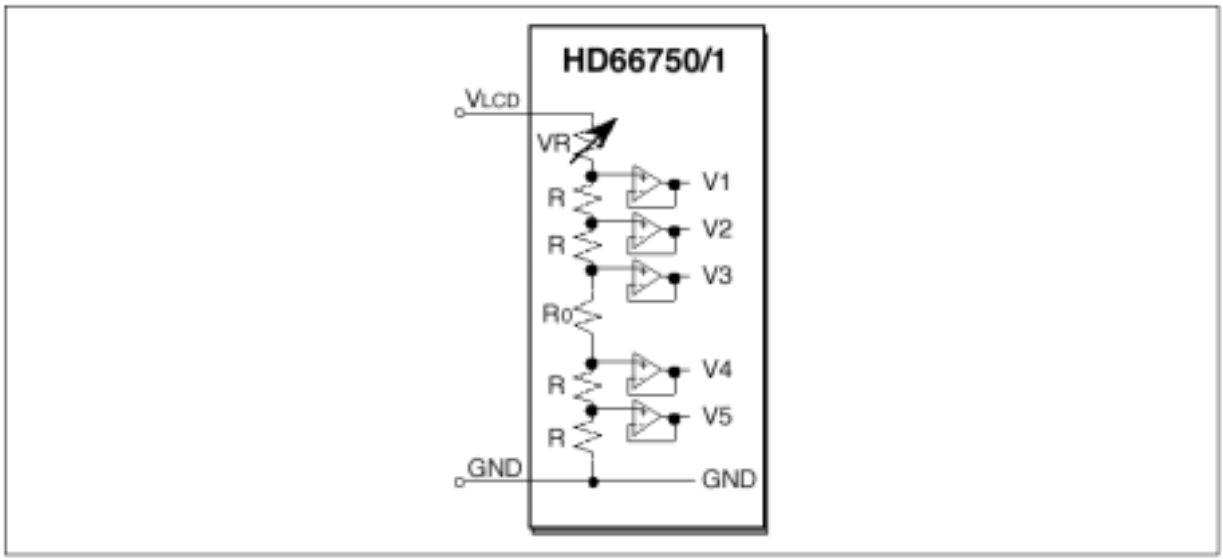
Power Control Instruction

Contrast Control

CT5–0: These bits control the LCD drive voltage (potential difference between V1 and GND) to adjust 64-step contrast. For details, see the Contrast Adjuster section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	*	*	*	*	*	*	*	*	*	*	**CT5**	**CT4**	**CT3**	**CT2**	**CT1**	**CT0**

Contrast Control Instruction



Contrast Adjuster

CT Bits and Variable Resistor Value of Contrast Adjuster

CT Set Value						
CT5	**CT4**	**CT3**	**CT2**	**CT1**	**CT0**	**Variable Resistor (VR)**
0	0	0	0	0	0	3.20 x R
0	0	0	0	0	1	3.15 x R
0	0	0	0	1	0	3.10 x R
0	0	0	0	1	1	3.05 x R
0	0	0	1	0	0	3.00 x R
			•			•
			•			•
0	1	1	1	1	1	1.65 x R
1	0	0	0	0	0	1.60 x R
1	0	0	0	0	1	1.55 x R
1	0	0	0	1	0	1.50 x R
			•			•
			•			•
1	1	1	1	0	1	0.15 x R
1	1	1	1	1	0	0.10 x R
1	1	1	1	1	1	0.05 x R

Entry Mode

Rotation

The write data sent from the microcomputer is modified in the HD66750S and written to the CGRAM. The display data in the CGRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

I/D: When I/D = 1, the address counter (AC) is automatically incremented by 1 after the data is written to the CGRAM. When I/D = 0, the AC is automatically decremented by 1 after the data is written to the CGRAM.

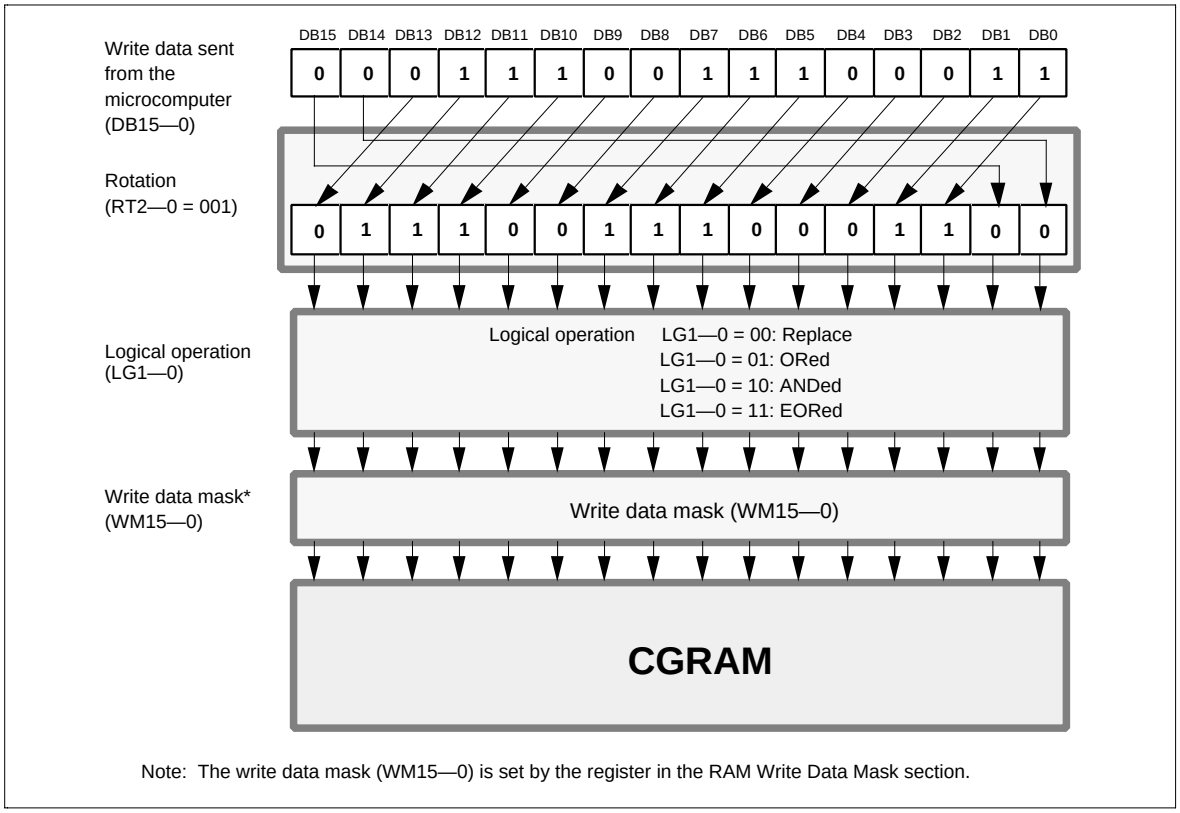
AM1–0: Set the automatic update method of the AC after the data is written to the CGRAM. When AM1–0 = 00, the data is continuously written in parallel. When AM1–0 = 01, the data is continuously written vertically. When AM1–0 = 10, the data is continuously written vertically with two-word width (32-bit length).

LG1–0: Write again the data read from the CGRAM and the data written from the microcomputer to the CGRAM by a logical operation. When LG1–0 = 00, replace (no logical operation) is done. ORed when LG1–0 = 01, ANDed when LG1–0 = 10, and EORed when LG1–0 = 11.

RT2–0: Write the data sent from the microcomputer to the CGRAM by rotating in a bit unit. RT3–0 specify rotation. For example, when RT2–0 = 001, the data is rotated in the upper side by two bits. When RT2–0 = 111, the data is rotated in the upper side by 14 bits. The upper bit overflown in the most significant bit (MSB) side is rotated in the least significant bit (LSB) side.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	*	*	*	*	*	*	*	*	*	*	*	**I/D**	**AM1**	**AM0**	**LG1**	**LG0**
0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	**RT2**	**RT1**	**RT0**

Entry Mode and Rotation Instruction



Note: The write data mask (WM15—0) is set by the register in the RAM Write Data Mask section.

Logical Operation and Rotation for the CGRAM

Display Control

PS1–0: When PS1–0 = 01, only the upper eight raster-rows (COM1–COM8) are fixed-displayed in vertical smooth scrolling, and the other display raster-rows are smooth-scrolled. When PS1–0 = 10, the upper 16 raster-rows (COM1–COM16) are fixed-displayed. When PS1–0 = 11, the upper 24 raster-rows (COM1–COM24) are fixed-displayed. For details, see the Partial Smooth Scroll Display Function section.

DHE: When DHE = 1, the double height between raster-rows specified in the Double-height Display Position section is displayed. For details, see the Double-height Display section.

GS: When GS = 0, the grayscale level at a weak-colored display (DB = 01) is 1/3. When GS = 1, the grayscale level at weak-colored display is 1/2, and at strong-colored display (when DB = 10) it is 2/3.

REV: Displays all character and graphics display sections with black-and-white reversal when REV = 1. For details, see the Reversed Display Function section.

D: Display is on when D = 1 and off when D = 0. When off, the display data remains in the CGRAM, and can be displayed instantly by setting D = 1. When D is 0, the display is off with the SEG1 to SEG128 outputs and COM1 to COM128 outputs set to the GND level. Because of this, the HD66750S can control the charging current for the LCD with AC driving.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	*	*	*	*	*	*	*	*	*	*	**PS1**	**PS0**	**DHE**	**GS**	**REV**	**D**

Display Control Instruction

Cursor Control

C: When C = 1, the window cursor display is started. The display mode is selected by the CM1–0 bits, and the display area is specified in a dot unit by the horizontal cursor position register (HS6–0 and HE6–0 bits) and vertical cursor position register (VS6–0 and VE6–0 bits). For details, see the Window Cursor Display section.

CM1–0: The display mode of the window cursor is selected. These bits can display a white-blink cursor, black-blink cursor, black-and-white reversed cursor, and black-and-white-reversed blink cursor.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	**C**	**CM1**	**CM0**

Cursor Control Instruction

CM Bits and Window Cursor Display Mode

CM1	CM0	Window Cursor Display Mode
0	0	White-blink cursor (alternately blinking between the normal display and an all-white display (all unlit))
0	1	Black-blink cursor (alternately blinking between the normal display and an all-black display (all lit))
1	0	Black-and-white reversed cursor (black-and-white-reversed normal display (no blinking))
1	1	Black-and-white-reversed blink cursor (alternately blinking the black-and-white-reversed normal display)

Double-height Display Position

DS6–0: Specify any common raster-row position where the double-height display starts. Note that no scrolling is done by vertical scrolling. For details, see the Double-height Display section.

DE6-0: Specify any common raster-row position where the double-height display ends. Set the end position of the double-height display after the start position of the double-height display, satisfying the relationship DS6–0 ≤ DE6–0. When the area specifying the double height has an odd number of raster-rows, the double-height display is done for the DE6–0 + 1 raster-rows.

When the double-height display is not used, set the DHE bit in the display-control instruction register to 0.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	*	DE6	DE5	DE4	DE3	DE2	DE1	DE0	*	DS6	DS5	DS4	DS3	DS2	DS1	DS0

Double-height Display Position Instruction

Vertical Scroll Control

SL6–0: Specify the display start raster-row for vertical smooth scrolling. Any raster-row from the first to 128th can be selected (table 14). After the 128th raster-row is displayed, the display restarts from the first raster-row. For details, see the Vertical Smooth Scroll section.

In partial smooth scrolling, these bits specify the display start raster-row of the next fixed-display raster-row. For details, see the Partial Smooth Scroll Display Function section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	*	*	*	*	*	*	*	*	*	SL6	SL5	SL4	SL3	SL2	SL1	SL0

Vertical Scroll Control Instruction

SL Bits and Display-start Raster-row

SL6	SL5	SL4	SL3	SL2	SL1	SL0	Display-start Raster-row
0	0	0	0	0	0	0	1st raster-row
0	0	0	0	0	0	1	2nd raster-row
0	0	0	0	0	1	0	3rd raster-row
0	0	0	0	0	1	1	4th raster-row
0	0	0	0	1	0	0	5th raster-row
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	127th raster-row
1	1	1	1	1	1	1	128th raster-row

Horizontal Cursor Position

Vertical Cursor Position

HS6-0: Specify the start position for horizontally displaying the window cursor in a dot unit. The cursor is displayed from the 'set value + 1' dot. Ensure that HS6–0 ≤ HE6–0.

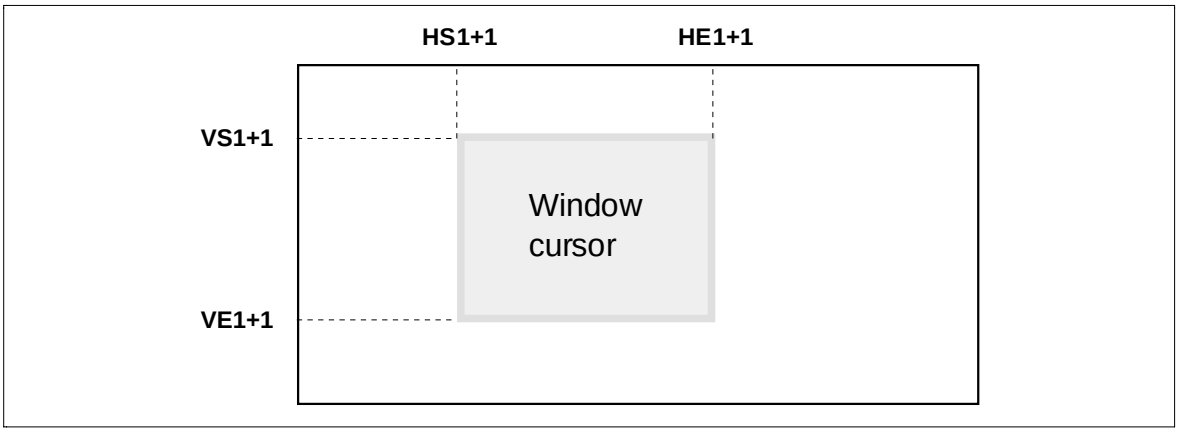
HE6-0: Specify the end position for horizontally displaying the window cursor in a dot unit. The cursor is displayed to the 'set value + 1' dot. Ensure that HS6–0 ≤ HE6–0.

VS6-0: Specify the start position for vertically displaying the window cursor in a dot unit. The cursor is displayed from the 'set value + 1' dot. Ensure that VS6–0 ≤ VE6–0.

VE6-0: Specify the end position for vertically displaying the window cursor in a dot unit. The cursor is displayed to the 'set value + 1' dot. Ensure that VS6–0 ≤ VE6–0. In vertical scrolling, rewrite VS6–0 and VE6–0 since this window cursor does not move vertically.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	*	HE6	HE5	HE4	HE3	HE2	HE1	HE0	*	HS6	HS5	HS4	HS3	HS2	HS1	HS0
0	1	*	VE6	VE5	VE4	VE3	VE2	VE1	VE0	*	VS6	VS5	VS4	VS3	VS2	VS1	VS0

Horizontal Cursor Position and Vertical Cursor Position Instruction



Window Cursor Position

RAM Write Data Mask

WM15-0: In writing to the CGRAM, these bits mask writing in a bit unit. When WM15 = 1, this bit masks the write data of DB15 and does not write to the CGRAM. Similarly, the WM14–0 bits mask the write data of DB14–0 in a bit unit. However, when AM = 10, the write data is masked with the set values of VM15–0 for the odd-times CGRAM write. It is also masked automatically with the reversed set values of VM15–0 for the even-times CGRAM write. For details, see the Graphics Operation Function section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	**VM 15**	**VM 14**	**VM 13**	**VM 12**	**VM 11**	**VM 10**	**VM 9**	**VM 8**	**VM 7**	**VM 6**	**VM 5**	**VM 4**	**VM 3**	**VM 2**	**VM 1**	**VM 0**

RAM Write Data Mask Instruction

RAM Address Set

AD10-0: Initially set CGRAM addresses to the address counter (AC). Once the CGRAM data is written, the AC is automatically updated according to the AM1–0 and I/D bit settings. This allows consecutive accesses without resetting addresses. Once the CGRAM data is read, the AC is not automatically updated. CGRAM address setting is not allowed in the sleep mode or standby mode.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	*	*	*	*	*	**AD 10**	**AD9**	**AD8**	**AD7**	**AD6**	**AD5**	**AD4**	**AD3**	**AD2**	**AD1**	**AD0**

RAM Address Set Instruction

AD Bits and CGRAM Setting

AD10–AD0	CGRAM Setting
"000"H–"00F"H	Bitmap data for COM1
"010"H–"01F"H	Bitmap data for COM2
"020"H–"02F"H	Bitmap data for COM3
"030"H–"03F"H	Bitmap data for COM4
:	:
"760"H–"76F"H	Bitmap data for COM119
"770"H–"77F"H	Bitmap data for COM120
"780"H–"78F"H	Bitmap data for COM121
"790"H–"79F"H	Bitmap data for COM122
"7A0"H–"7AF"H	Bitmap data for COM123
"7B0"H–"7BF"H	Bitmap data for COM124
"7C0"H–"7CF"H	Bitmap data for COM125
"7D0"H–"7DF"H	Bitmap data for COM126
"7E0"H–"7EF"H	Bitmap data for COM127
"7F0"H–"7FF"H	Bitmap data for COM128

Write Data to CGRAM

WD15-0 : Write 16-bit data to the CGRAM. After a write, the address is automatically updated according to the AM1–0 and I/D bit settings. During the sleep and standby modes, the CGRAM cannot be accessed.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	**WD 15**	**WD 14**	**WD 13**	**WD 12**	**WD 11**	**WD 10**	**WD 9**	**WD 8**	**WD 7**	**WD 6**	**WD 5**	**WD 4**	**WD 3**	**WD 2**	**WD 1**	**WD 0**

Write Data to CGRAM Instruction

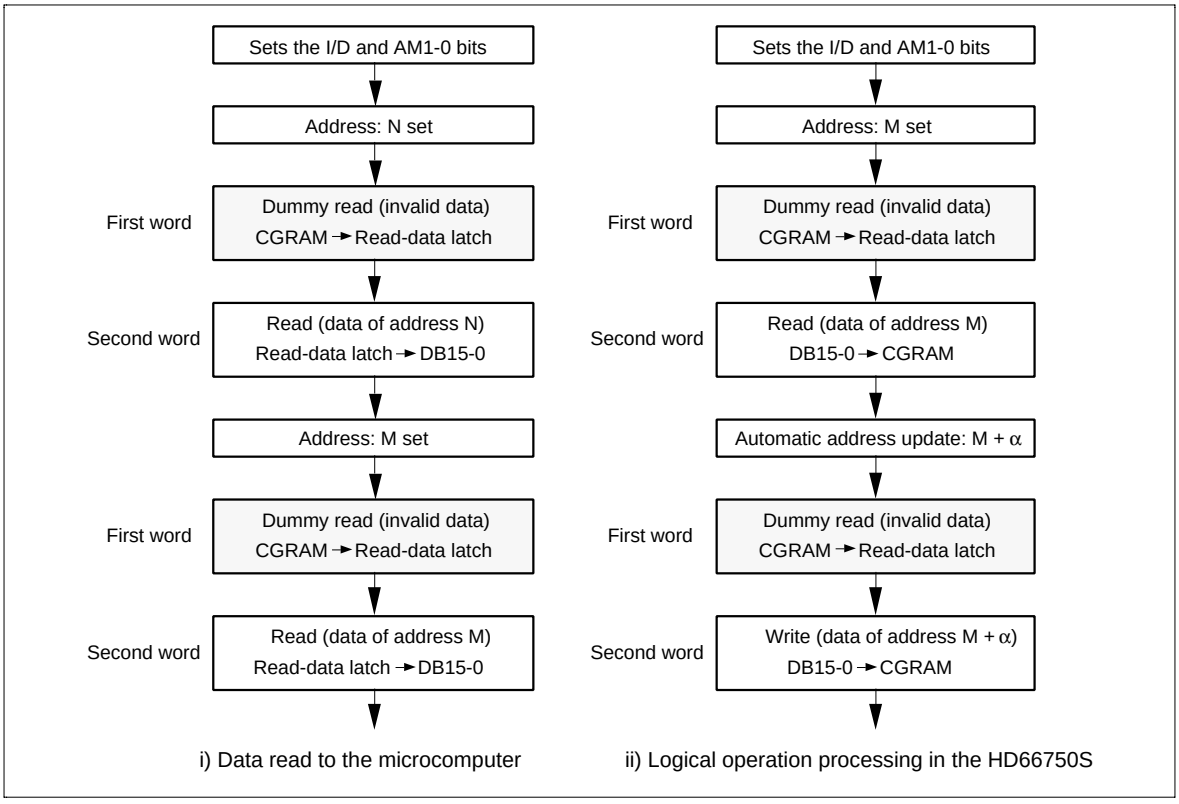
Read Data from CGRAM

RD15-0 : Read 16-bit data from the CGRAM. When the data is read to the microcomputer, the first-word read immediately after the CGRAM address setting is latched from the CGRAM to the internal read-data latch. The data on the data bus (DB15–0) becomes invalid and the second-word read is normal.

When bit processing, such as a logical operation, is performed within the HD66750S, only one read can be processed since the latched data in the first word is used.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	**RD 15**	**RD 14**	**RD 13**	**RD 12**	**RD 11**	**RD 10**	**RD 9**	**RD 8**	**RD 7**	**RD 6**	**RD 5**	**RD 4**	**RD 3**	**RD 2**	**RD 1**	**RD 0**

Read Data from CGRAM Instruction



CGRAM Read Sequence

4.3 CGRAM Address Map

Relationship Between Display Position and CGRAM Address

Segment Driver		SEG1/128	SEG2/127	SEG3/126	SEG4/125	SEG5/124	SEG6/123	SEG7/122	SEG8/121	SEG9/120	.. SEG16/113	SEG17/112	.. SEG24/105	.....	SEG121/8	.. SEG128/1
Bit	SGS="0"	D0 D1	D2 D3	D4 D5	D6 D7	D8 D9	D10 D11	D12 D13	D14 D15	D0 D1	.. D15	D0 D1	.. D15	.....	D0 D1	.. D15
	SGS="1"	D15 D14	D13 D12	D11 D10	D9 D8	D7 D6	D5 D4	D3 D2	D1 D0	D15 D14	.. D0	D15 D14	.. D0	.....	D15 D14	.. D0
COM1		Address: "000"H								"001"H		"002"H		.....	"00F"H	
COM2		Address: "010"H								"011"H		"012"H		.....	"01F"H	
COM3		Address: "020"H								"021"H		"022"H		.....	"02F"H	
COM4		Address: "030"H								"031"H		"032"H		.....	"03F"H	
COM5		Address: "040"H								"041"H		"042"H		.....	"04F"H	
COM6		Address: "050"H								"051"H		"052"H		.....	"05F"H	
COM7		Address: "060"H								"061"H		"062"H		.....	"06F"H	
COM8		Address: "070"H								"071"H		"072"H		.....	"07F"H	
COM9		Address: "080"H								"081"H		"082"H		.....	"08F"H	
COM10		Address: "090"H								"091"H		"092"H		.....	"09F"H	
COM11		Address: "0A0"H								"0A1"H		"0A2"H		.....	"0AF"H	
COM12		Address: "0B0"H								"0B1"H		"0B2"H		.....	"0BF"H	
COM13		Address: "0C0"H								"0C1"H		"0C2"H		.....	"0CF"H	
COM14		Address: "0D0"H								"0D1"H		"0D2"H		.....	"0DF"H	
COM15		Address: "0E0"H								"0E1"H		"0E2"H		.....	"0EF"H	
COM16		Address: "0F0"H								"0F1"H		"0F2"H		.....	"0FF"H	
COM17		Address: "100"H								"101"H		"102"H		.....	"10F"H	
COM18		Address: "110"H								"111"H		"112"H		.....	"11F"H	
COM19		Address: "120"H								"121"H		"122"H		.....	"12F"H	
COM20		Address: "130"H								"131"H		"132"H		.....	"13F"H	
⋮		⋮								⋮		⋮		.....	⋮	
COM125		Address: "7C0"H								"7C1"H		"7C2"H		.....	"7CF"H	
COM126		Address: "7D0"H								"7D1"H		"7D2"H		.....	"7DF"H	
COM127		Address: "7E0"H								"7E1"H		"7E2"H		.....	"7EF"H	
COM128		Address: "7F0"H								"7F1"H		"7F2"H		.....	"7FF"H	

Relationship between CGRAM Data and Display Contents

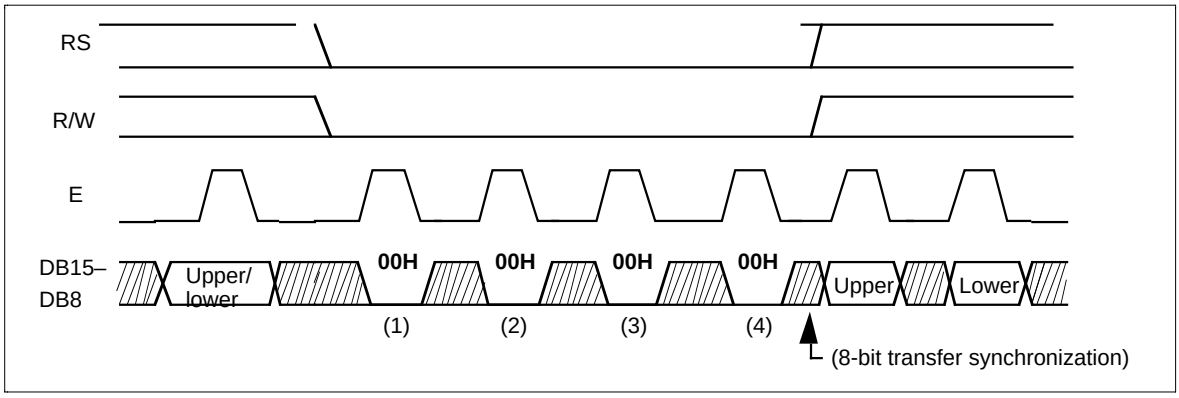
Upper bit	Lower bit	LCD
0	0	Non-selection display (unlit)
0	1	1/3 or 1/2 level grayscale display (selected by the GS bit)
1	0	2/3 level gray scale
1	1	Selection display (lit)

Note : Upper bits: DB15, DB13, DB11, DB9, DB7, DB5, DB3, DB1
Lower bits: DB14, DB12, DB10, DB8, DB6, DB4, DB2, DB0

4.4 Graphics Operation Function

8-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/GND/Vcc level allows 68-system E-clock-synchronized 8-bit parallel data transfer using pins DB15–DB8. Setting the IM2/1/0 to the GND/Vcc/Vcc level allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins DB7–DB0 to the Vcc or GND level.



8-bit Transfer Synchronization

Note: Transfer synchronization function for an 8-bit bus interface
The HD66750S supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a 00H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.

The module can greatly reduce the load of the microcomputer graphics software processing through the 16-bit bus architecture and graphics-bit operation function. This function supports the following：

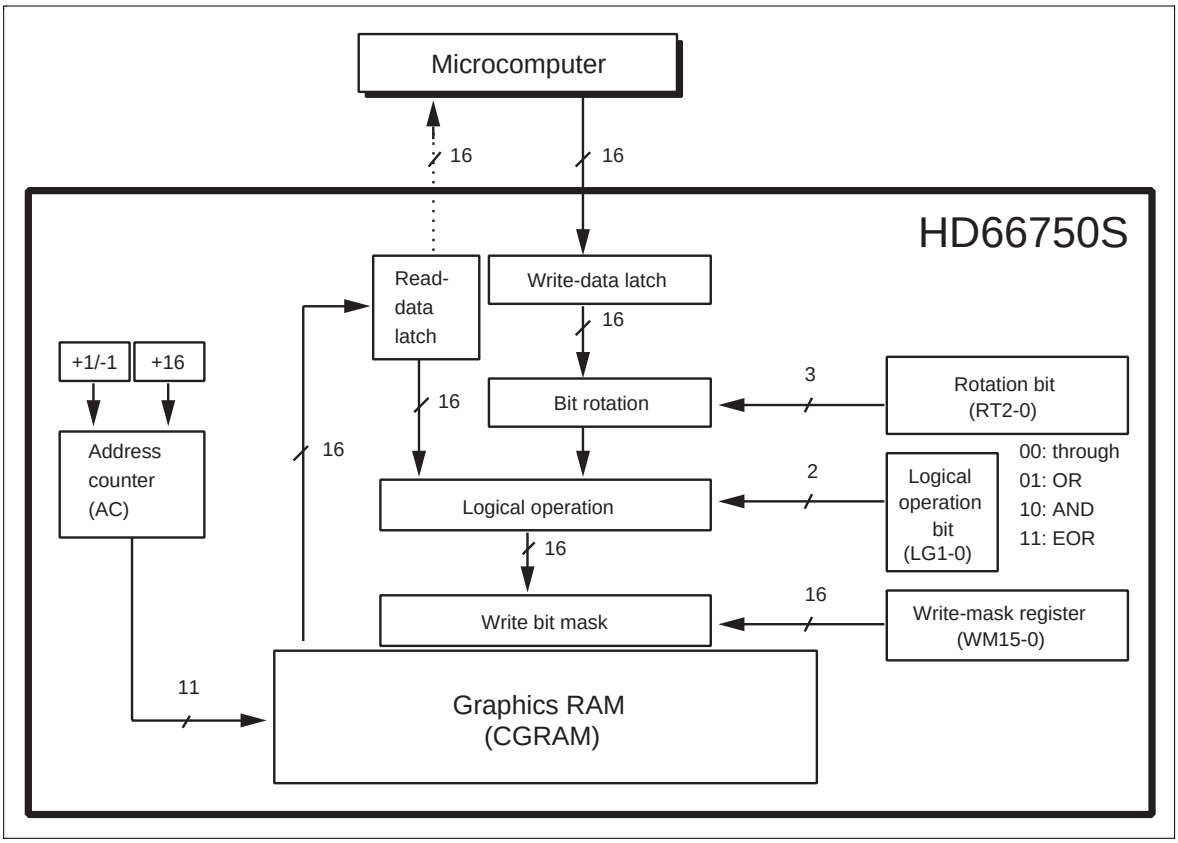
1. A write data mask function that selectively rewrite some of the bits in the 16-bit write data.
2. A bit rotation function that shifts and writes the data sent from the microcomputer in a bit unit.
3. A logical operation function that writes the data sent from the microcomputer and the original RAM data by a logical operation.

Since the display data in the graphics RAM （CGRAM）can be quickly rewritten，the load of the microcomputer processing can be reduced in the large display screen when a font pattern，such as kanji characters，is developed for any position （BiTBLT processing）.

The graphics bit operation can be controlled by combining the entry mode register，the bit set value of the RAM-write-data mask register，and the read/write from the microcomputer.

Graphics Operation

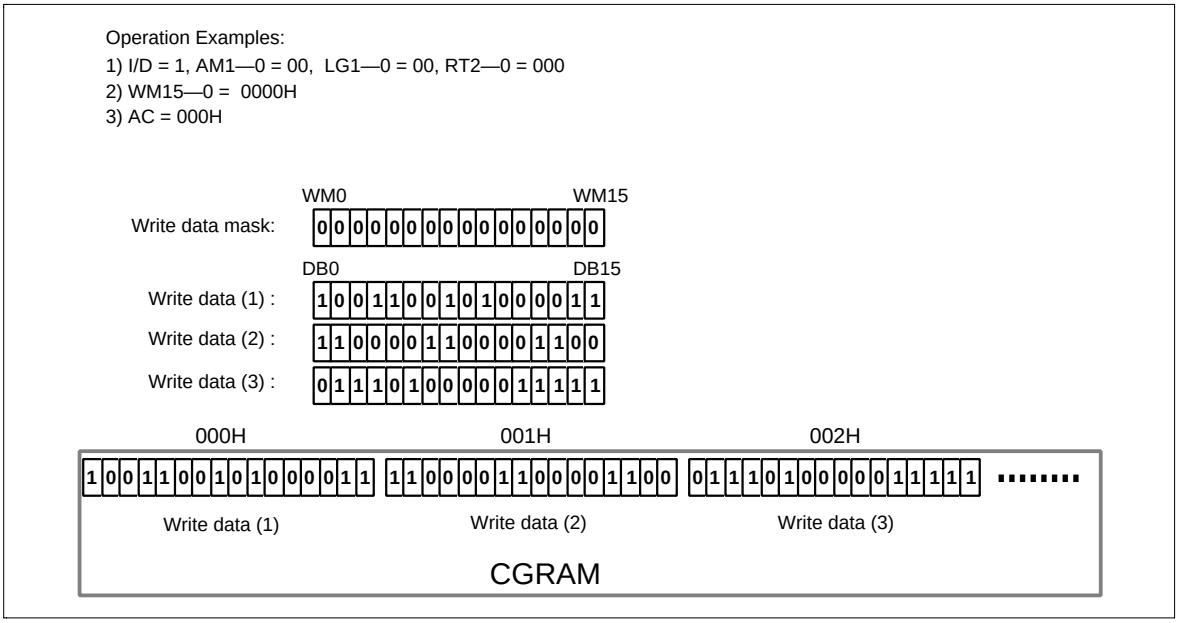
	Bit Setting			
Operation Mode	**I/D**	**AM**	**LG**	**Operation and Usage**
Write mode 1	0/1	00	00	Horizontal data replacement, horizontal-border drawing
Write mode 2	0/1	01	00	Vertical data replacement, font development, vertical-border drawing
Write mode 3	0/1	10	00	Vertical data replacement with two-word width, kanji-font development
Read/write mode 1	0/1	00	01 10 11	Horizontal data replacement with logical operation, horizontal-border drawing
Read/write mode 2	0/1	01	01 10 11	Vertical data replacement with logical operation, vertical-border drawing
Read/write mode 3	0/1	10	01 10 11	Horizontal data replacement with two-word-width logical operation



Data Processing Flow of the Graphics Bit Operation

1. Write mode 1: AM1–0 = 00, LG1–0 = 00

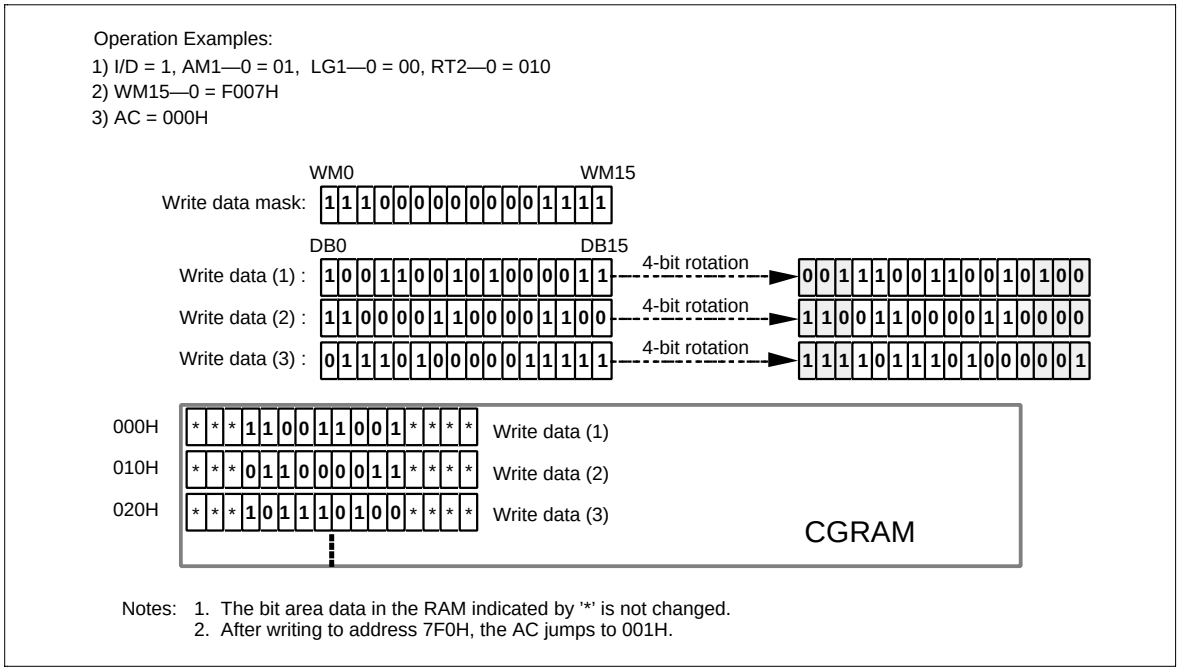
This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (CGRAM) or to draw borders. The rotation function (RT2–0) or write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left edge of the graphics RAM.



Writing Operation of Write Mode 1

2. Write mode 2: AM1–0 = 01, LG1–0 = 00

This mode is used when the data is vertically written at high speed. It can also be used to initialize the graphics RAM (CGRAM), develop the font pattern in the vertical direction, or draw borders. The rotation function (RT2–0) or write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 16, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the graphics RAM.

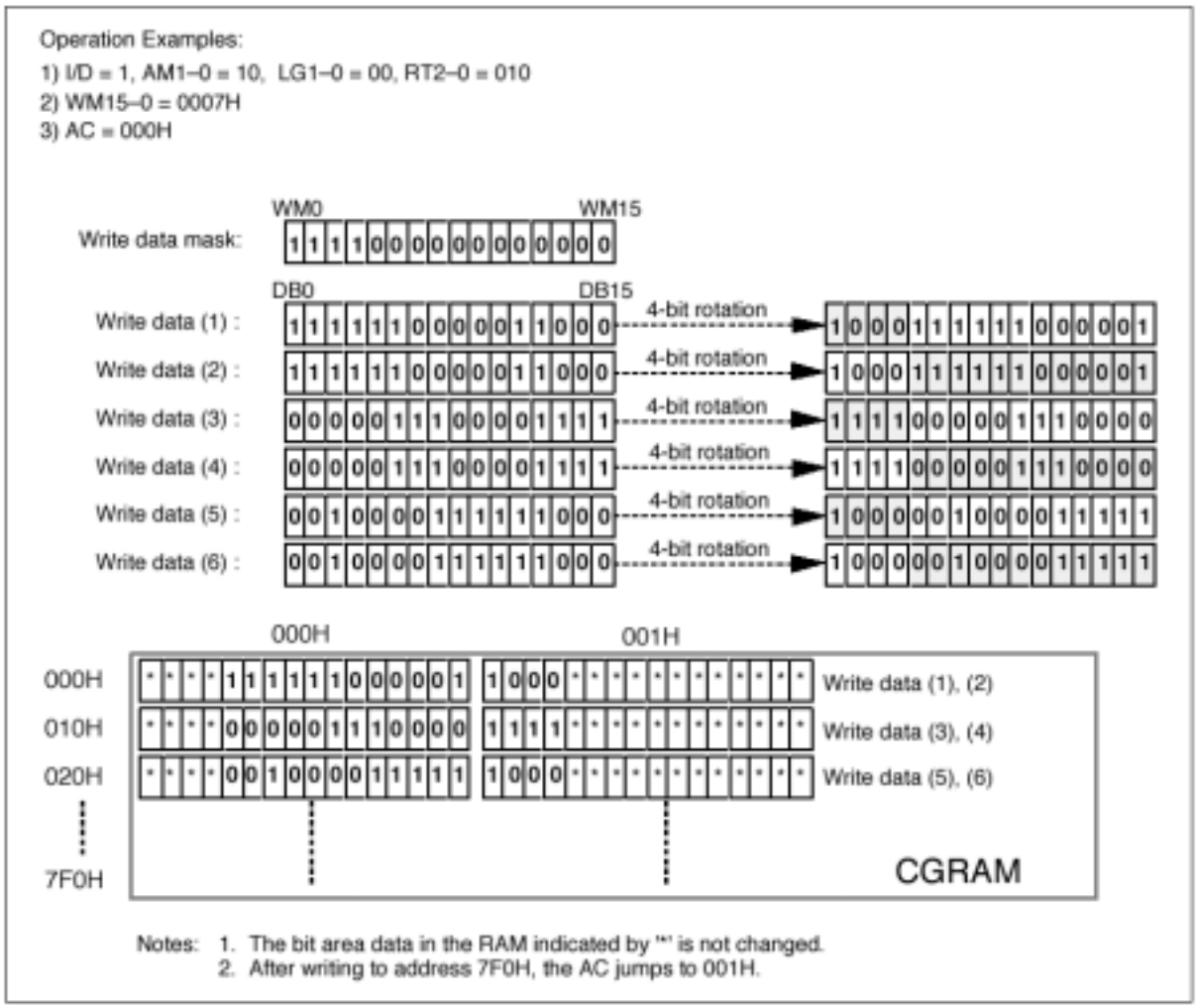


Notes: 1. The bit area data in the RAM indicated by '*' is not changed.
2. After writing to address 7F0H, the AC jumps to 001H.

Writing Operation of Write Mode 2

3. Write mode 3: AM1–0 = 10, LG1–0 = 00

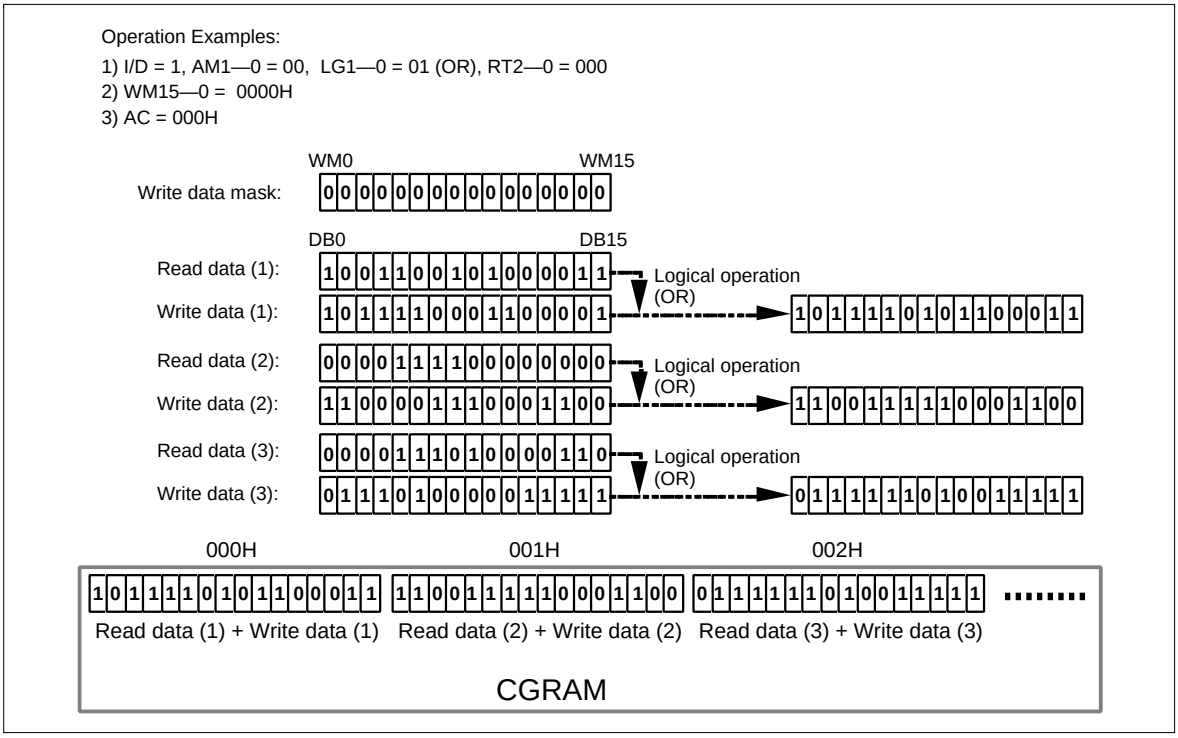
This mode is used when the data is written at high speed by vertically shifting bits. It can also be used to write the 16-bit data for two words into the graphics RAM (CGRAM), develop the font pattern, or transfer the BiTBLT as a bit unit. The rotation function (RT2–0) or write-data mask function (WM15–0) are also enabled in these operation. However, although the write-data mask function masks the bit position set with the write-data mask register (WM15–0) at the odd-times (such as the first or third) write, the function masks the bit position that reversed the setting value of the write-data mask register (WM15–0) at the even-times (such as the second or fourth) write. After the odd-times writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0). After the even-times writing, the AC automatically increments or decrements by –1 + 16 (I/D = 1) or +1 + 16 (I/D = 0). The AC automatically jumps to the upper edge after it has reached the lower edge of the graphics RAM.



Writing Operation of Write Mode 3

4. Read/Write mode 1: AM1–0 = 00, LG1–0 = 01/10/11

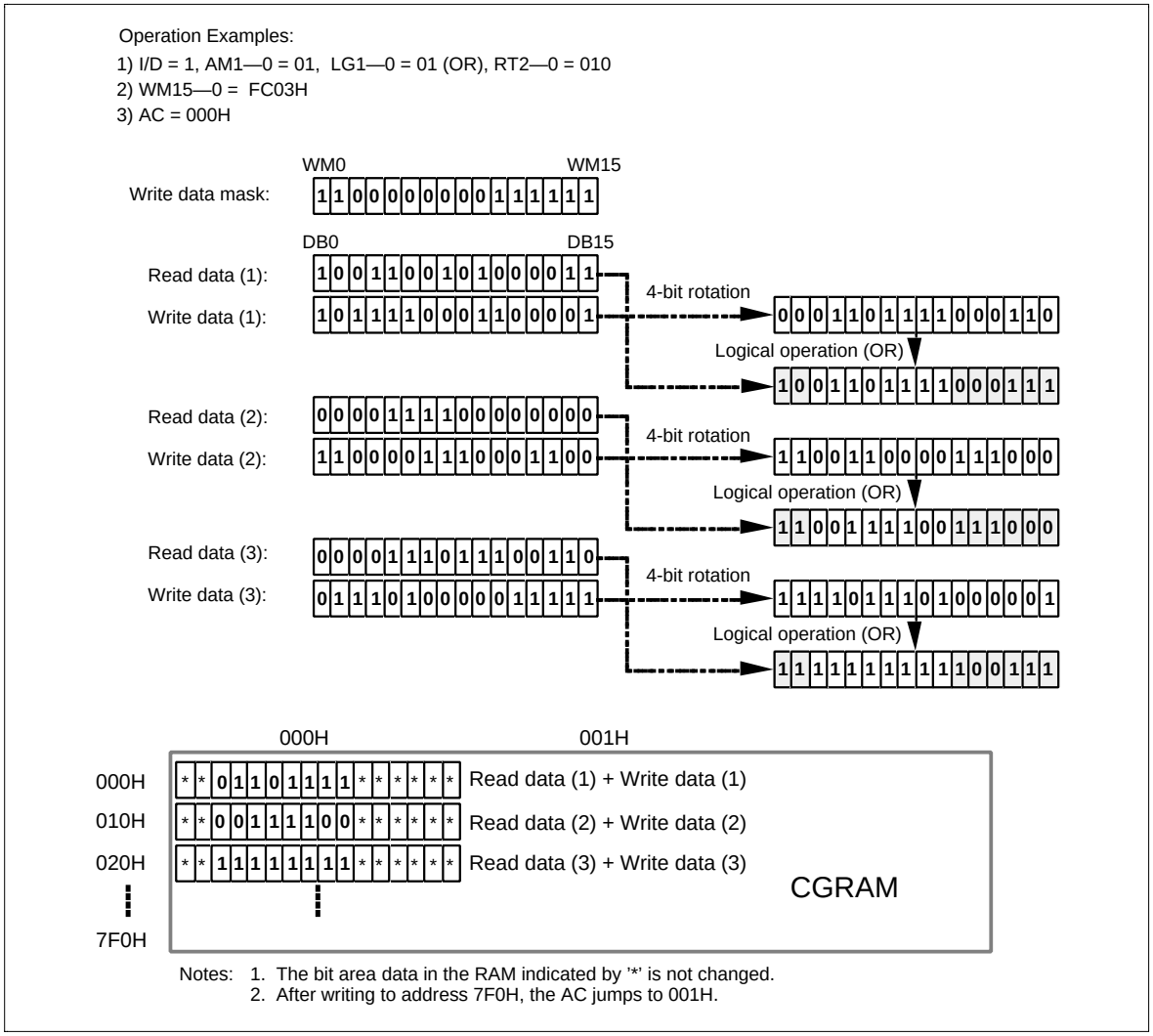
This mode is used when the data is horizontally written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the graphics RAM (CGRAM), performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the CGRAM. This mode can read the data during the same bus cycle as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. The rotation function (RT2–0) or write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the graphics RAM.



Writing Operation of Read/Write Mode 1

5. Read/Write mode 2: AM1–0 = 01, LG1–0 = 01/10/11

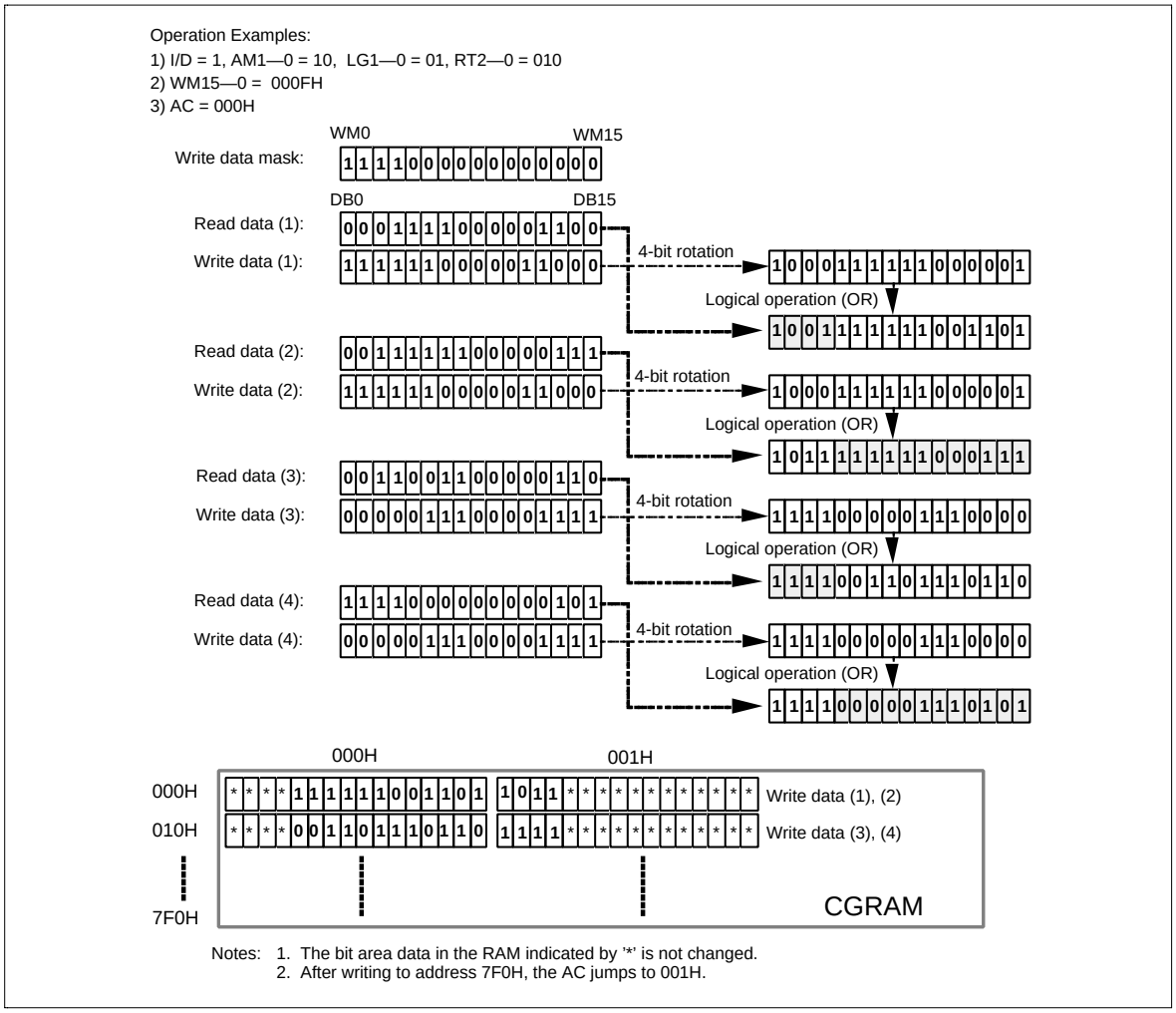
This mode is used when the data is vertically written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the graphics RAM (CGRAM), performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the CGRAM. This mode can read the data during the same bus cycle as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. The rotation function (RT2–0) or write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 16, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the graphics RAM.



Writing Operation of Read/Write Mode 2

6. Read/Write mode 3: AM1–0 = 10, LG1–0 = 01/10/11

This mode is used when the data is written with high speed by vertically shifting bits and by performing logical operation with the original data. It can be also used to write the 16-bit data for two words into the graphics RAM (CGRAM), develop the font pattern, or transfer the BiTBLT as a bit unit. This mode can read the data during the same bus cycle as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. The rotation function (RT2–0) or write-data mask function (WM15–0) are also enabled in these operations. However, although the write-data mask function masks the bit position set with the write-data mask register (WM15–0) at the odd-times (such as the first or third) write, the function masks the bit position which reversed the setting value of the write-data mask register (WM15–0) at the even-times (such as the second or fourth) write. After the odd-times writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0). After the even-times writing, the AC automatically increments or decrements by –1 + 16 (I/D = 1) or +1 + 16 (I/D = 0). The AC automatically jumps to the upper edge after it has reached the lower edge of the graphics RAM.



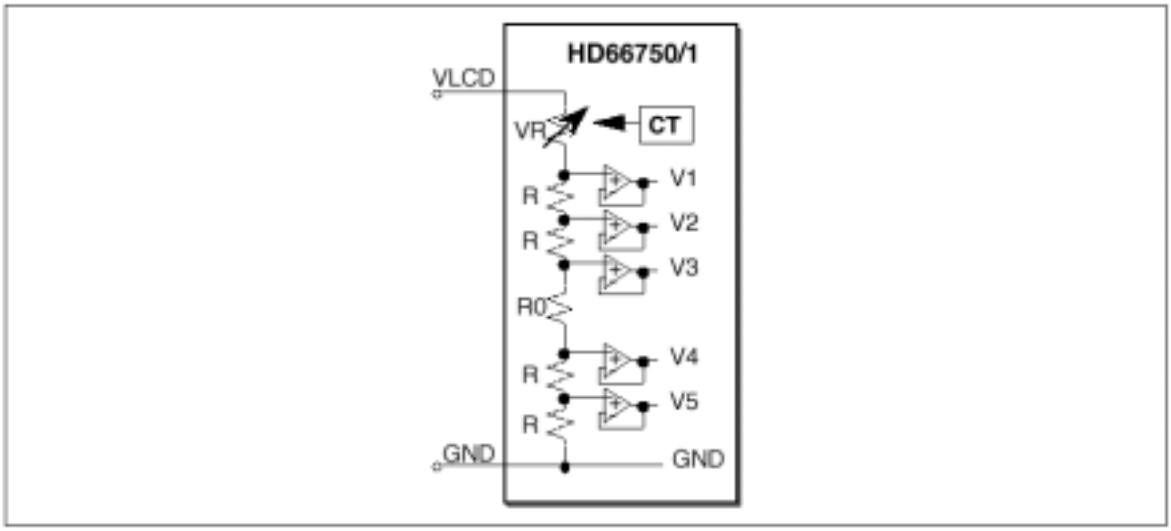
Notes: 1. The bit area data in the RAM indicated by '*' is not changed.
2. After writing to address 7F0H, the AC jumps to 001H.

Writing Operation of Read/Write Mode 3

4.5 Contrast Adjuster Function

Software can adjust 64-step contrast for an LCD by varying the liquid-crystal drive voltage (potential difference between V_{LCD} and V1) through the CT bits of the contrast adjustment register (electron volume function). The value of a variable resistor between V_{LCD} and V1 (VR) can be precisely adjusted in a 0.05 x R unit within a range from 0.05 x R through 3.20 x R, where R is a reference resistance obtained by dividing the total resistance.

The HD66750/1 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder resistors, which generate different liquid-crystal drive voltages. Thus, CT5-0 bits must be adjusted so that potential difference between V_{LCD} and V1 is 0.1 V or higher and that between V4 and GND is 1.4 V or higher when liquid-crystal drives, particularly when the VR is small.



Contrast Adjuster

Contrast Adjustment Bits （CT）and Variable Resistor Values

CT set value						Variable Resistor Value (VR)	Potential Difference between V1 and GND	Display Color
CT5	CT4	CT3	CT2	CT1	CT0			
0	0	0	0	0	0	3.20 x R	(Small)	(Light)
0	0	0	0	0	1	3.15 x R	:	:
0	0	0	0	1	0	3.10 x R	:	:
0	0	0	0	1	1	3.05 x R	:	:
0	0	0	1	0	0	3.00 x R	:	:
0	0	0	1	0	1	2.95x R	:	:
0	0	0	1	1	0	2.90 x R	:	:
0	0	0	1	1	1	2.85 x R	:	:
0	0	1	0	0	0	2.80 x R	:	:
0	0	1	0	0	1	2.75 x R	:	:
0	0	1	0	1	0	2.70 x R	:	:
0	0	1	0	1	1	2.65x R	:	:
0	0	1	1	0	0	2.60 x R	:	:
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1.65 x R	:	:
1	0	0	0	0	0	1.60 x R	:	:
1	0	0	0	0	1	1.55 x R	:	:
1	0	0	0	1	0	1.50 x R	:	:
1	0	0	0	1	1	1.45 x R	:	:
1	0	0	1	0	0	1.40 x R	:	:
1	0	0	1	0	1	1.35 x R	:	:
1	0	0	1	1	0	1.30 x R	:	:
1	0	0	1	1	1	1.25 x R	:	:
1	0	1	0	0	0	1.20 x R	:	:
1	0	1	0	0	1	1.15 x R	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	0	0	0.20 x R	:	:
1	1	1	1	0	1	0.15 x R	:	:
1	1	1	1	1	0	0.10 x R	:	:
1	1	1	1	1	1	0.05 x R	(Large)	(Deep)

4.6 Four-grayscale Display Function

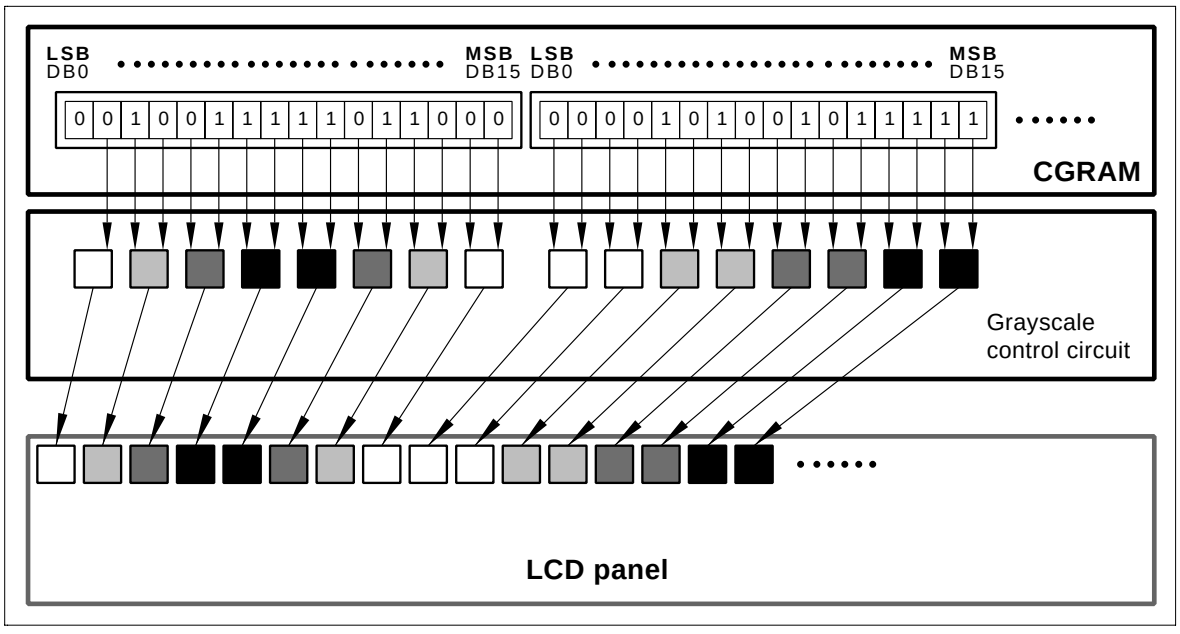
The HD66750S supports the four-grayscale monochrome display function. The four-grayscale monochrome display is used for the display data of the two-bit pixel set sent to the CGRAM. There are four grayscale levels: always unlit, weak middle level, strong middle level, and always lit. In the weak middle-level grayscale display, the GS bit can select the 1/3 or 1/2 level.

The frame rate control (FRC) method is used for grayscale control.

Relationships between the CGRAM Data and the Display Contents

Upper Bit	Lower Bit	Liquid Crystal Display
0	0	Non-selected (unlit)
0	1	GS = 0: 1/3-level grayscale (one frame lit during a three-frame period)
		GS = 1: 1/2-level grayscale (one frame lit during a two-frame period)
1	0	2/3-level grayscale (two frames lit during a three-frame period)
1	1	Selected (lit)

Note: Upper bits: DB15, DB13, DB11, DB9, DB7, DB5, DB3, and DB1
Lower bits: DB14, DB12, DB10, DB8, DB6, DB4, DB2, and DB0



Four-grayscale Monochrome Display

4.7 Window Cursor Display Function

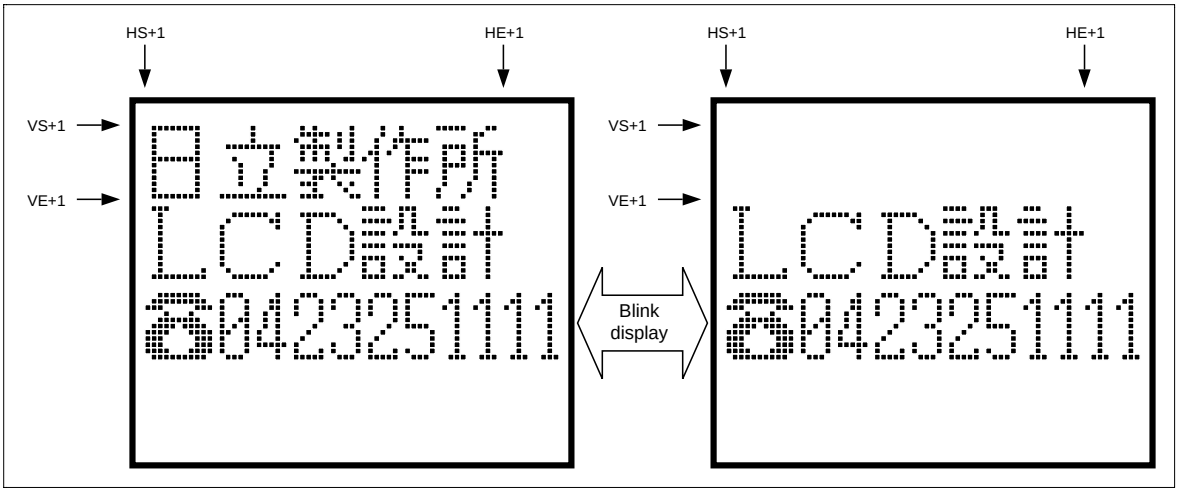
The HD66750S displays the window cursor by specifying a window area. The horizontal display position of the window cursor is specified with the horizontal cursor position register (HS6-0 to HE6-0), and the vertical display position is specified with the vertical cursor position register (VS6-0 or VE6-0). In these display position setting registers, ensure that HS6-0 ≤ HE6-0 and VS6-0 ≤ VE6-0. If these relationships are not satisfied, normal display cannot be attained. In addition, if the setting is VS6-0 = VE6-0 = 00H, a cursor is displayed on a raster-row at the most-upper edge of the screen.

This window cursor can automatically display the hardware-supported block cursor, highlight window, or menu bar. The CM1-0 bits select the following four displays in each window cursor:

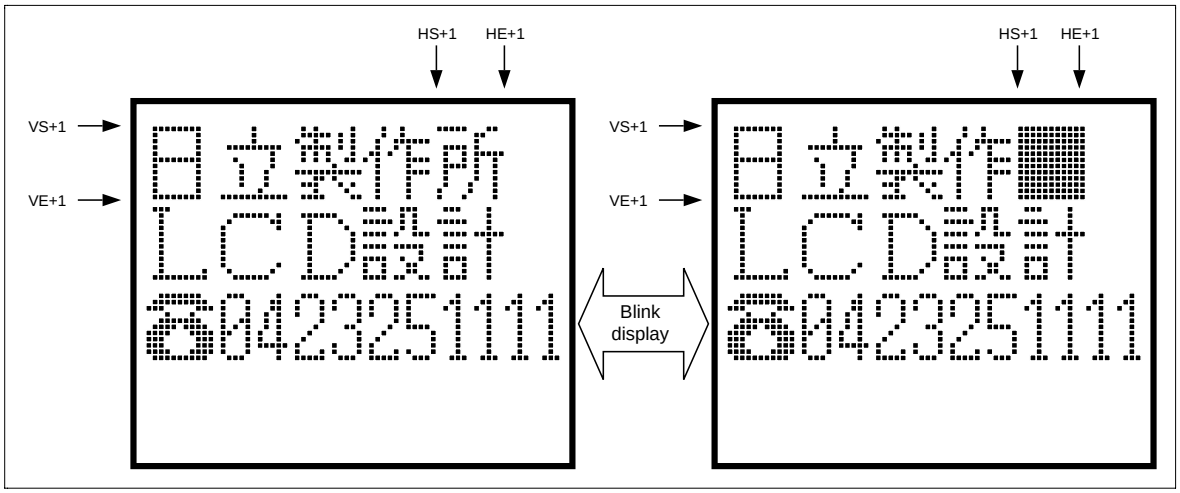
1. White-blink cursor (CM1-0 = 00): Alternately blinks between the normal display and an all-white (unlit) display
2. Black-blink cursor (CM1-0 = 01): Alternately blinks between the normal display and an all-black (all lit) display
3. Black-and-white reversed cursor (CM1-0 = 10): Black-and-white-reversed normal display (no blinking)
4. Black-and-white-reversed blink cursor (CM1-0 = 11): Alternately blinks between the normal display and a black-and-white-reversed display

The above blinking display is switched in a 32-frame unit.

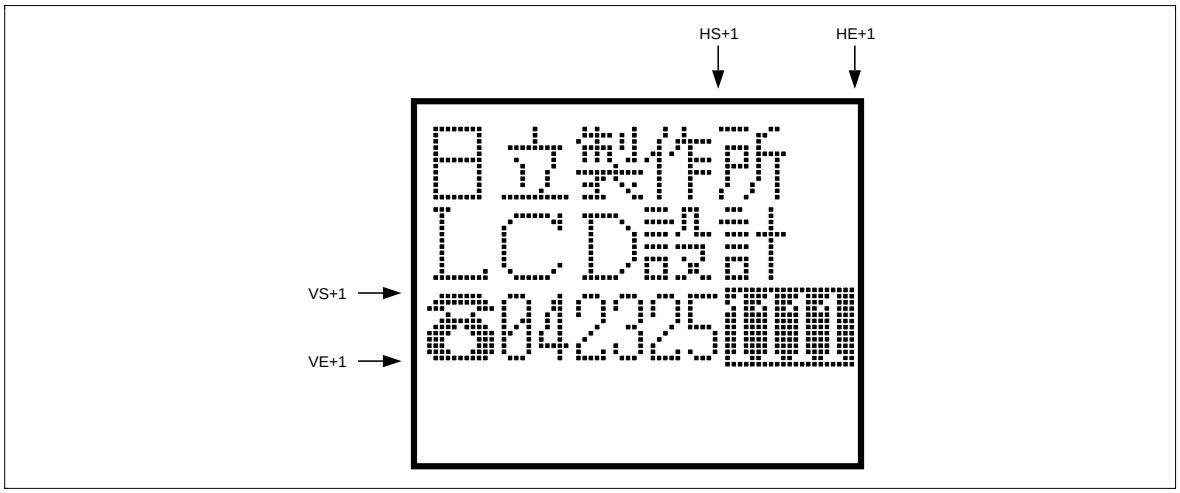
In vertical scrolling, note that this window cursor does not automatically move vertically.



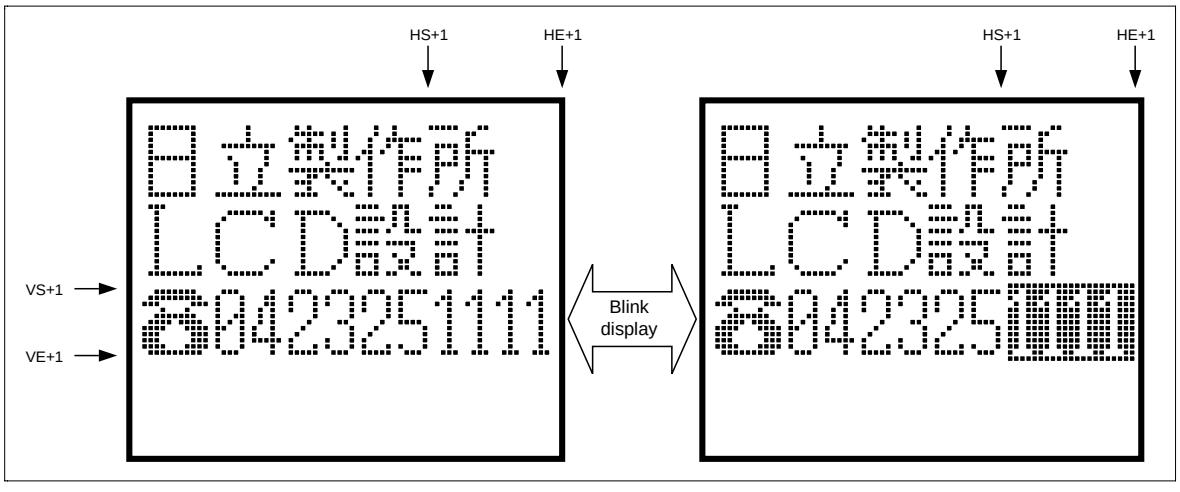
White Blink Cursor Display



Black Blink Cursor Display



Black-and-white Reversed Cursor Display



Black-and-white Reversed Blink Cursor Display

4.8 Vertical Smooth Scroll Function

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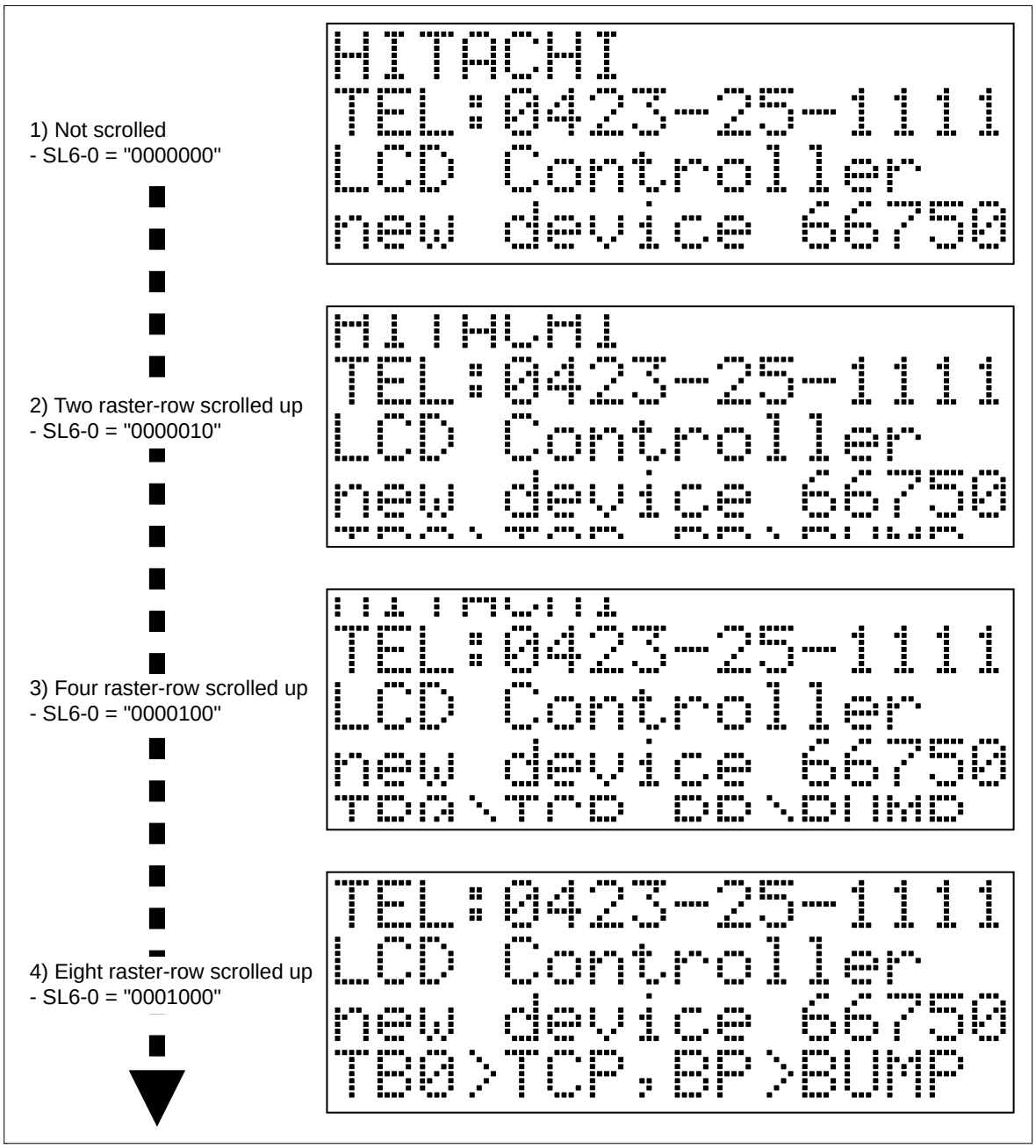
The HD66750S can scroll the graphics display vertically in units of raster-rows. The data storage capacity of the CGRAM is 128 raster-rows. Continuous smooth vertical scrolling is achieved by writing display data into a raster-row area that is not being used for display. After the 128th raster-row is displayed, the first raster-row is displayed again. Using the status read, the user can check the display raster-rows (L6-0) that are currently driving the LCD, and flicker can be eliminated by writing the display data in the CGRAM while the LCD is not driven.

Additionally, when display areas of a graphics icon such as a pictogram or a menu bar are partially fixed-displayed, the remaining areas can be displayed. For details, see the Partial Smooth Scroll Display Function section.

Specifically, this function is controlled by incrementing or decrementing the value in the display-start raster-row bits (SL6-0) by 1. For example, to smoothly scroll up, increment display-start raster-row bits (SL6-0) by 1 from 0000000 to 1111111 to scroll 128 raster-rows.

Note that the vertical double-height display or window cursor display is not automatically changed in synchronization with the vertical scrolling.

When the response speed of the liquid crystal is low or when high-speed scrolling is needed, two- to four-raster-row scrolling is recommended.



Vertical Smooth Scroll

4.9 Partial Smooth Scroll Display Function

The HD66750S can partially fixed-display the areas of a graphics icon such as a pictogram or a menu bar, and perform vertical smooth scrolling of the remaining bit-map areas. Since the PS1 to PS0 bits are not used for smooth scrolling of the upper first to 24th display raster-rows but are used for fixed-display, pictograms can be placed on the screen. This function can largely control the rewrite frequencies of the bit-map data during smooth scrolling and reduce the software load of the MPU.

Bit Setting and Display Lines

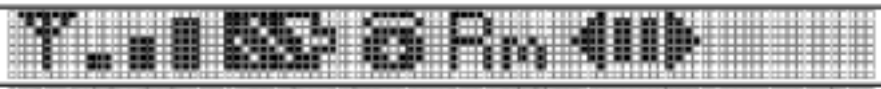
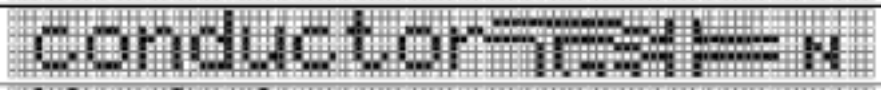
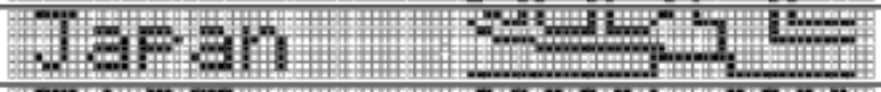
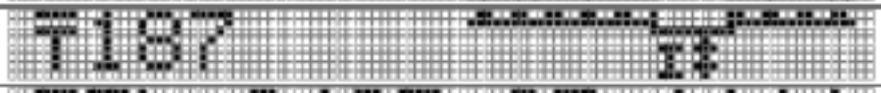
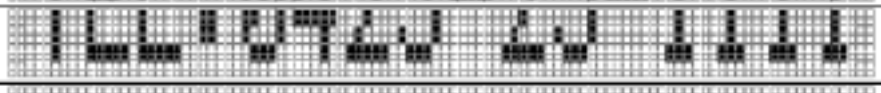
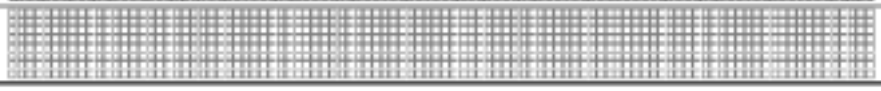
Bit Setting	COM Position	SL6-0 =00H	SL6-0 =01H	SL6-0 =02H	SL6-0 =04H	SL6-0 =07H	SL6-0 =08H		SL6-0 =7EH	SL6-0 =7FH
PS1-0 = "00"	COM1	1st raster-row	2nd raster-row	3rd raster-row	5th raster-row	8th raster-row	9th raster-row	• • •	127th raster-row	128th raster-row
		2nd raster-row	3rd raster-row	4th raster-row	6th raster-row	9th raster-row	10th raster-row	• • •	128th raster-row	1st raster-row
		3rd raster-row	4th raster-row	5th raster-row	7th raster-row	10th raster-row	11th raster-row	• • •	1st raster-row	2nd raster-row
		•	•	•	•	•	•		•	•
		•	•	•	•	•	•		•	•
		•	•	•	•	•	•		•	•
		118th raster-row	119th raster-row	120th raster-row	122nd raster-row	125th raster-row	126th raster-row	• • •	116th raster-row	117th raster-row
		119th raster-row	120th raster-row	121st raster-row	123rd raster-row	126th raster-row	127th raster-row	• • •	117th raster-row	118th raster-row
	COM120	120th raster-row	121 raster-row	122nd raster-row	124th raster-row	127th raster-row	128th raster-row	• • •	118th raster-row	119th raster-row
PS1-0 = "01"	COM1	1st to 8th raster-row	1st to 8th raster-row	1st to 8th raster-row	1st to 8th raster-row	1st to 8th raster-row	1st to 8th raster-row	• • •	1st to 8th raster-row	1st to 8th raster-row
		1st raster-row	2nd raster-row	3rd raster-row	5th raster-row	8th raster-row	9th raster-row	• • •	127th raster-row	128th raster-row
		2nd raster-row	3rd raster-row	4th raster-row	6th raster-row	9th raster-row	10th raster-row	• • •	128th raster-row	9th raster-row
		3rd raster-row	4th raster-row	5th raster-row	7th raster-row	10th raster-row	11th raster-row		9th raster-row	10th raster-row
		•	•	•	•	•	•		•	•
		•	•	•	•	•	•		•	•
		110th raster-row	111th raster-row	112th raster-row	114th raster-row	117th raster-row	118th raster-row	• • •	116th raster-row	117th raster-row
		111th raster-row	112th raster-row	113th raster-row	115th raster-row	118th raster-row	119th raster-row	• • •	117th raster-row	118th raster-row
	COM120	112th raster-row	113th raster-row	114th raster-row	116th raster-row	119th raster-row	120th raster-row	• • •	118th raster-row	119th raster-row
PS1-0 = "10"	COM1	1st to 16th raster-row	1st to 16th raster-row	1st to 16th raster-row	1st to 16th raster-row	1st to 16th raster-row	1st to 16th raster-row	• • •	1st to 16th raster-row	1st to 16th raster-row
		1st raster-row	2nd raster-row	3rd raster-row	5th raster-row	8th raster-row	9th raster-row	• • •	127th raster-row	128th raster-row
		2nd raster-row	3rd raster-row	4th raster-row	6th raster-row	9th raster-row	10th raster-row	• • •	128th raster-row	17th raster-row
		3rd raster-row	4th raster-row	5th raster-row	7th raster-row	10th raster-row	11th raster-row		17th raster-row	18th raster-row
		•	•	•	•	•	•		•	•
		•	•	•	•	•	•		•	•
		102nd raster-row	103rd raster-row	104th raster-row	106th raster-row	109th raster-row	110th raster-row	• • •	116th raster-row	117th raster-row
		103rd raster-row	104th raster-row	105th raster-row	107th raster-row	110th raster-row	111th raster-row	• • •	117th raster-row	118th raster-row
	COM120	104th raster-row	105th raster-row	106th raster-row	108th raster-row	111th raster-row	112nd raster-row	• • •	118th raster-row	119th raster-row
PS1-0 = "11"	COM1	1st to 24th raster-row	1st to 24th raster-row	1st to 24th raster-row	1st to 24th raster-row	1st to 24th raster-row	1st to 24th raster-row	• • •	1st to 24th raster-row	1st to 24th raster-row
		1st raster-row	2nd raster-row	3rd raster-row	5th raster-row	8th raster-row	9th raster-row	• • •	127th raster-row	128th raster-row
		2nd raster-row	3rd raster-row	4th raster-row	6th raster-row	9th raster-row	10th raster-row	• • •	128th raster-row	25th raster-row
		3rd raster-row	4th raster-row	5th raster-row	7th raster-row	10th raster-row	11th raster-row		25th raster-row	26th raster-row
		•	•	•	•	•	•		•	•
		•	•	•	•	•	•		•	•
		94th raster-row	95th raster-row	96th raster-row	98th raster-row	101th raster-row	102th raster-row	• • •	116th raster-row	117th raster-row
		95th raster-row	96th raster-row	97th raster-row	99th raster-row	102th raster-row	103th raster-row	• • •	117th raster-row	118th raster-row
	COM120	96th raster-row	97th raster-row	98th raster-row	100th raster-row	103th raster-row	104nd raster-row	• • •	118th raster-row	119th raster-row

Notes: 1. The shadow raster-rows above are fixed-displayed. They do not depend on the setting of the SL6-0 bits.

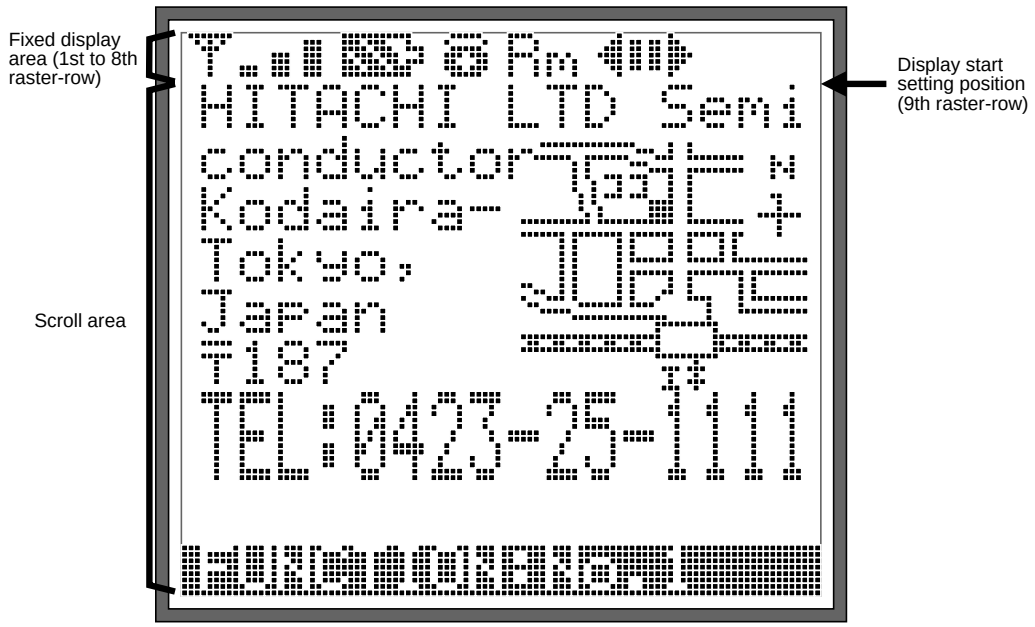
2. The SL6-0 bits specify the next first scroll display raster-row of the fixed-displayed raster-rows.

Partial Smooth Scroll Display Examples

Data Setting to the CGRAM

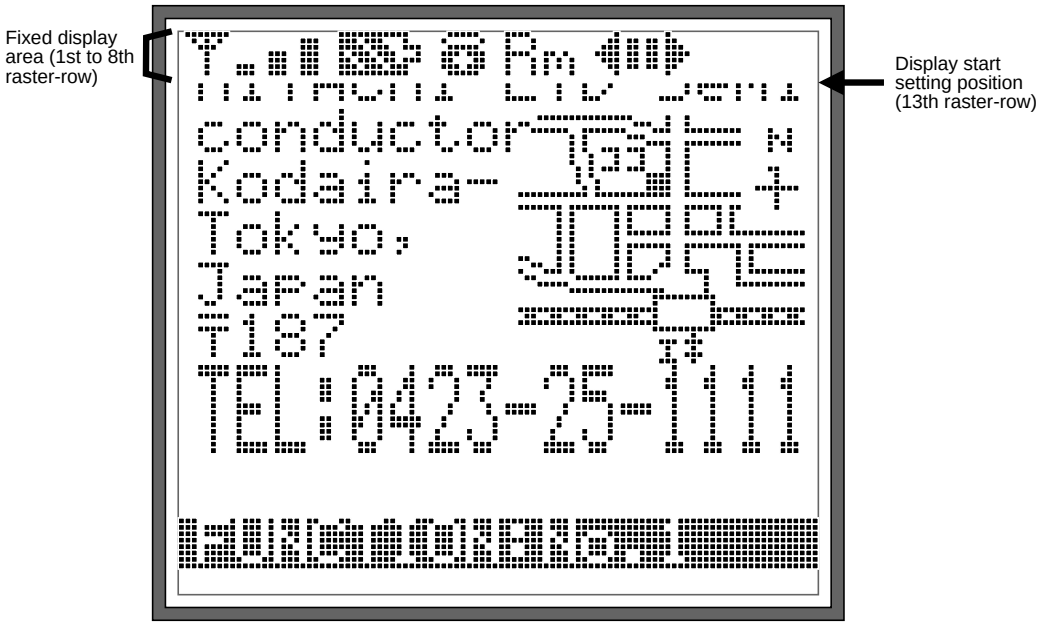
CGRAM Address	CGRAM Data
000 to 07F	
080 to 0FF	
100 to 17F	
180 to 1FF	
200 to 27F	
280 to 2FF	
300 to 37F	
380 to 3FF	
400 to 47F	
480 to 4FF	
500 to 57F	
580 to 5FF	

i) Initial screen display
- PS1-0 = "01" : Fixed-displays the first to eighth raster-rows
- SL6-0 = "0001000" : Starts display from the ninth raster-row



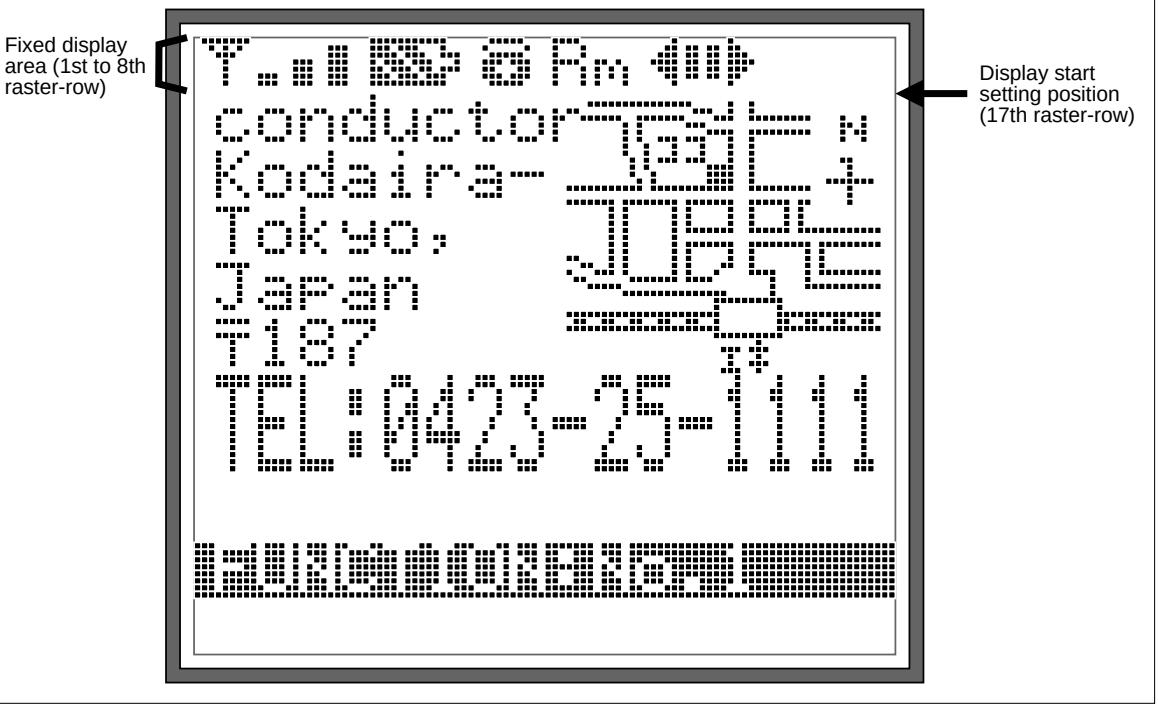
Example of Initial Screen in the Partial Smooth Scroll Mode

ii) Four-dot partial scroll up
- PS1-0 = "01" : Fixed-displays the first to eighth raster-rows
- SL6-0 = "0001100" : Starts display from the 13th raster-row



Example of Initial Screen in the Partial Smooth Scroll Mode （1）

iii) Eight-dot partial scroll up
- PS1-0 = "01" : Fixed-displays the first to eighth raster-rows
- SL6-0 = "0010000" : Starts display from the 17th raster-row



Example of Initial Screen in the Partial Smooth Scroll Mode （2）

4.10 Double-height Display Function

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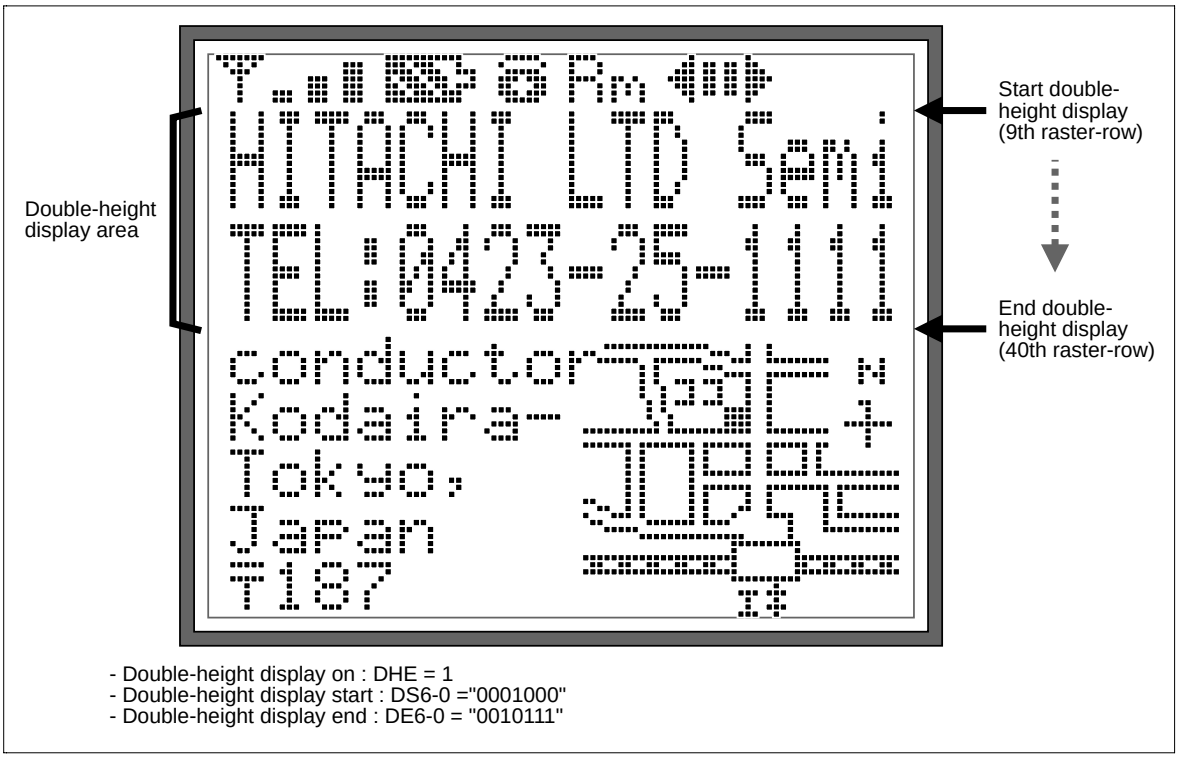
The HD66750S can double the height of any desired area in units of raster-rows (dots). The double-height display is done by setting the DHE bit in the display control register to 1.

The start position of the double-height display is set by the DS6 to DS0 bits of the double-height display position register, and the double-height display starts at the (the setting value plus one)-th raster-row. The end position is set by the DE6 to DE0 bits of the double-height display position register, and the display ends at the (the setting value plus one)-th raster-row. Here, the end position of the double-height display must be after the start position, so set the register setting values so that
DS6-0 ≤ DE6-0. When the area specified to be doubled in height is an odd number of raster-rows, the double-height display is done up to the (DE6-0 plus one)-th raster-row.

In vertical smooth scrolling, the double-height display position does not automatically move up or down.



Double-height Display（9th to 40th raster-rows）

4.11 Reversed Display Function

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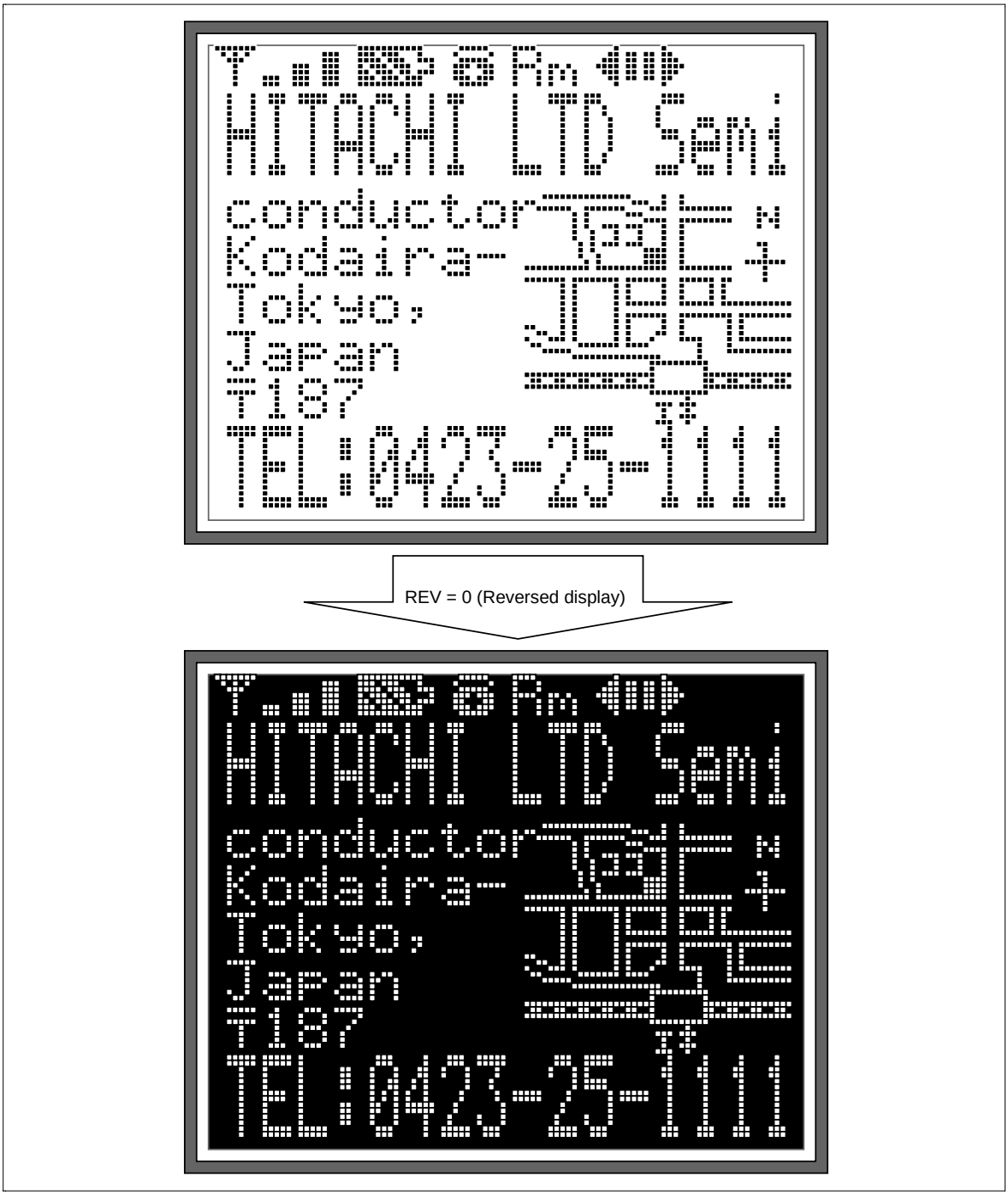
The HD66750S can display graphics display sections by black-and-white reversal. Black-and-white reversal can be easily displayed when the REV bit in the display control register is set to 1.



4.12 Partial-display-on Function

The HD66750S can program the liquid crystal display drive duty ratio setting (NL3-0 bits), the liquid crystal display drive bias value selection (BS2-0 bits), the boost output level selection (BT1-0 bits), and the contrast adjustment (CT5-0 bits). For example, when the 128 x 120-dot screen is normally displayed with a 1/120 duty ratio, the HD66750S can selectively drive only the center of the screen or the top of the screen by combining these register functions and the centering display function (CN bit). This is called partial-display-on. Lowering the liquid crystal display drive duty ratio reduces the liquid crystal display drive voltage, thus reducing internal current consumption. This is suitable for a 16 raster-row display (1/16 duty ratio) of a calendar or time in the system-standby state, or the display of only graphics icons (pictograms) at the top of the screen, which enables continuous display with minimal current consumption. The non-displayed lines are constantly driven by the unselected level voltage, thus turning off the LCD for these lines.

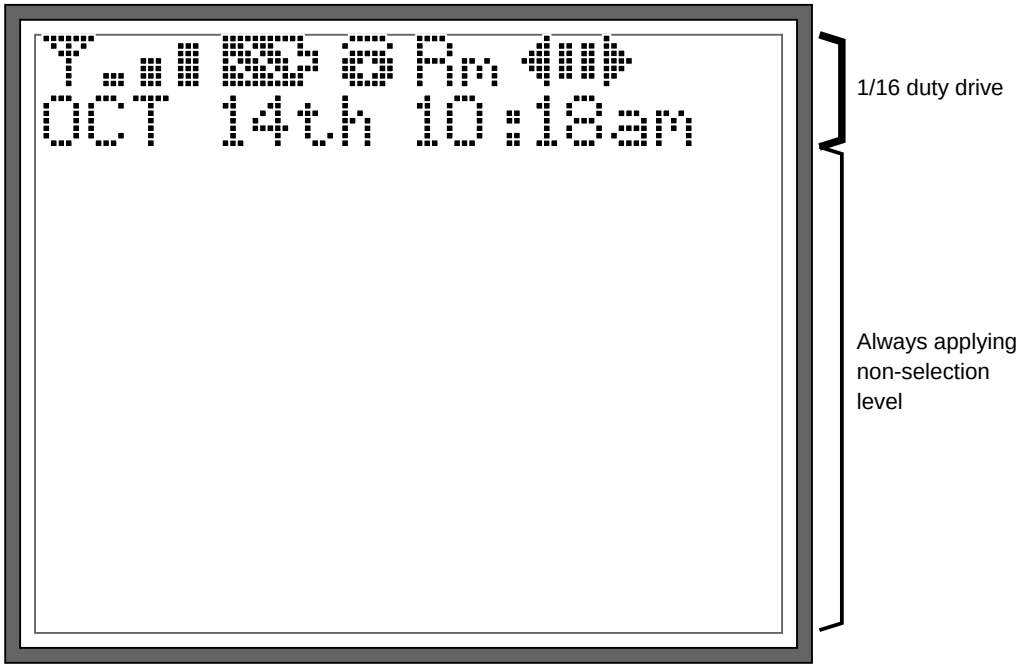
In general, lowering the liquid crystal display drive duty ratio decreases the optimum liquid crystal display drive voltage and liquid crystal display drive bias value. This reduces output multiplying factors in the booster and greatly controls current consumption.

Partial-display-on Function (1/120-duty Normal Drive)

Item	Normal Display	Partial-on Display (Limited to Four-line Display)	
LCD screen	128 x 120 dots	128 x 16 dots only on the center of the screen	128 x 16 dots only at the top of the screen
LCD drive position shift	Not necessary (CN = 0)	Necessary (CN = 1)	Not necessary (CN = 0)
LCD drive duty ratio	1/120 (NL3 to 0 = 1110)	1/16 (NL3 to 0 = 0001)	1/16 (NL3 to 0 = 0001)
LCD drive bias value (optimum)	1/11 (BS2 to 0 = 000)	1/5 (BS2 to 0 = 110)	1/5 (BS2 to 0 = 110)
LCD drive voltage*	13.5 V to 15.5 V (precisely adjustable using CT5 to 0)	4 V to 5 V (precisely adjustable using CT5 to 0)	4 V to 5 V (precisely adjustable using CT5 to 0)
Boosting output multiplying factor	Six times (BT1 to 0 = 10)	Two times (BT1 to 0 = 00)	Two times (BT1 to 0 = 00)
Frame frequency (fosc = 70 kHz)	68 Hz	68 Hz	68 Hz

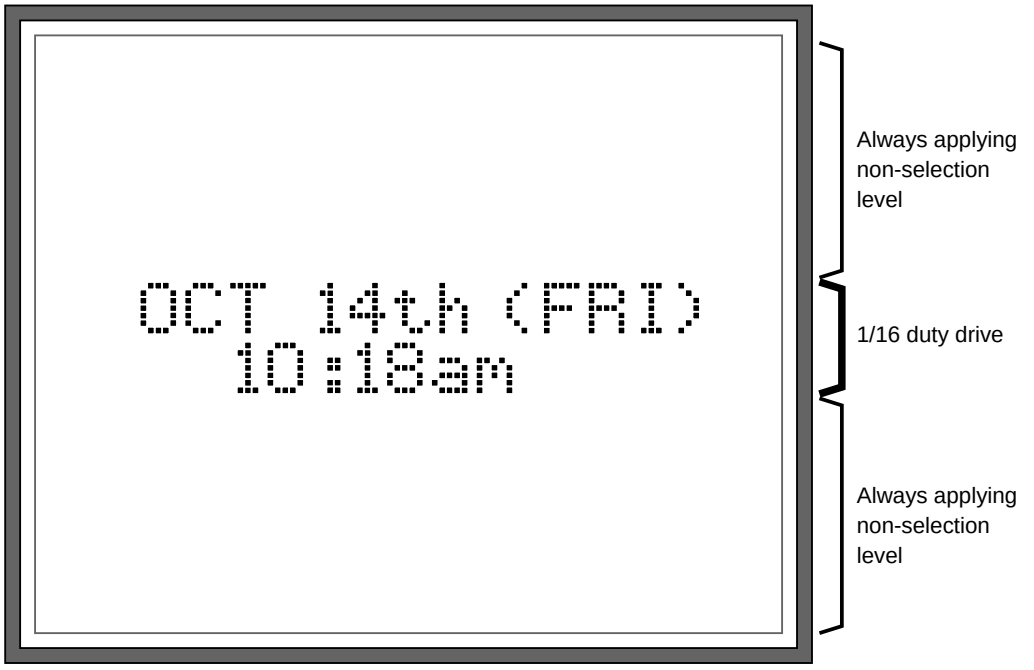
Note: The LCD drive voltage depends on the LCD materials used. Since the LCD drive voltage is high when the LCD drive duty ratio is high, a low duty ratio enables low-power consumption.

i) 1/16 duty drive at the top of the screen



Partial-on display （Date and Time Indicated） （1）

ii) 1/16 duty drive at the center of the screen (Centering display)



Partial-on display （Date and Time Indicated） （2）

4.13 Sleep and Standby Function

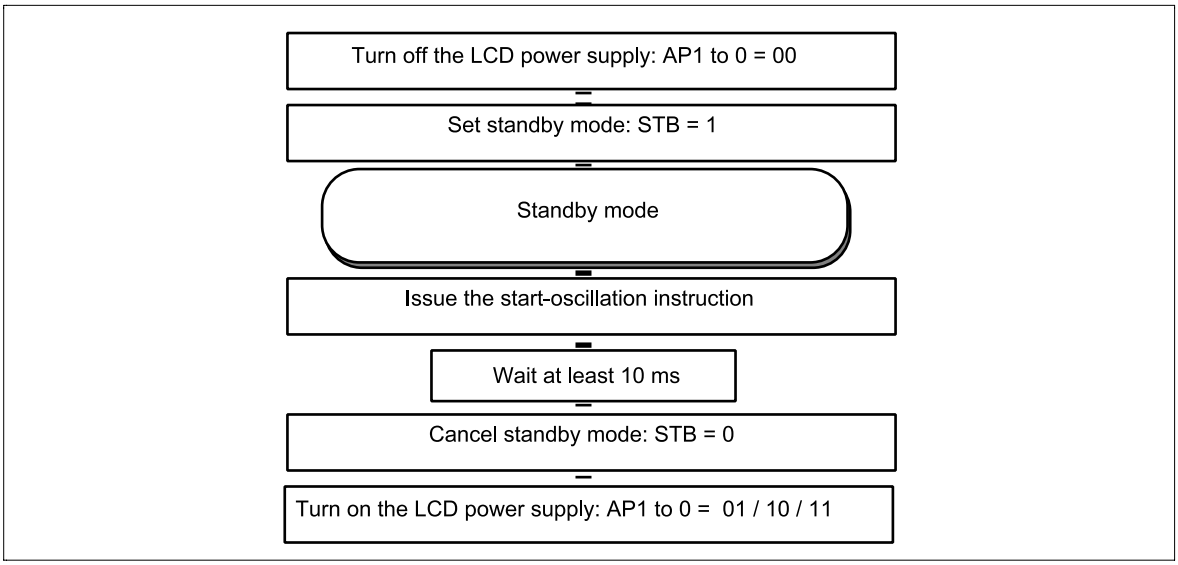
Setting the sleep mode bit (SLP) to 1 puts the HD66750S in the sleep mode, where the device stops all internal display operations, thus reducing current consumption. Specifically, LCD operation is completely halted. Here, all the SEG (SEG1 to SEG128) and COM (COM1 to COM128) pins output the GND level, resulting in no display. If the AP1-0 bits in the power control register are set to 00 in the sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

Comparison of Sleep Mode and Standby Mode

Function	Sleep Mode (SLP = 1)	Standby Mode (STB = 1)
LCD control	Turned off	Turned off
R-C oscillation circuit	Operates normally	Operation stopped

Setting the standby mode bit (STB) to 1 puts the HD66750S in the standby mode, where the device stops completely, halting all internal operations including the R-C oscillation circuit, thus further reducing current consumption compared to that in the sleep mode. Specifically, all the SEG (SEG1 to SEG128) and COM (COM1 to COM128) pins for the multiplexing drive output the GND level, resulting in no display. If the AP1-0 bits are set to 00 in the standby mode, the LCD drive power supply can be turned off.

During the standby mode, no instructions can be accepted other than the start-oscillation instruction. To cancel the standby mode, issue the start-oscillation instruction to stabilize R-C oscillation before setting the STB bit to 0.



Procedure for Setting and Canceling Standby Mode

5. Reliability

5.1 Environmental Test

Item No	Items	Content of Test	Test Condition	Applicable Standard
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	80°C 200 Hrs	
2	Low temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C 200Hrs	
3	High temperature operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time	70°C 200Hrs (*1)	
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 200Hrs (*1)	
5	High temperature / humidity storage	Endurance test applying the high temperature and high humidity storage for a long time.	40°C 90% RH 200Hrs	
6	Temperature cycle	Endurance test applying the low and high temperature cycles. -30°C ⟷ 80°C (30min.) (30min.) 1 Cycle	10 Cycle.	
7	Vibration test	10 → 55 → 10 Hz, within 1 minute amplitude 1.5mm .	15 minutes for each direction(X,Y,Z)	
8	Drop test	Packed, 100CM free fall, (6 sides, 1corner, 3edges)		

***1) : Driving condition for operation test:**

Power supply voltage for logic system =＋3.0V

Power supply voltage for LCD system = Getting Optimum Contrast at 25°C

6. HANDLING INSTRUCTION

☐ PRECAUTION IN USE OF LCD

- Do not contact or scratch the front surface and the contact pads of an LCD panel with hard materials such as metal or glass or with one‘s nail.
- To clean the surface,wipe it gently with soft cloth dampened alcohol.
- Do not attempt to wiped off the contact pads.
- Keep LCD panels away from direct sunlight,also avoid storing them in a high-temperature&high humidity environment for a long period.
- Do not drive LCD panels by DC voltage.
- Do not expose LCD panels to organic solvent.
- Liquid in LCD is hazardous substance, any contacts with liquid crystal materials ,wash it off immediately with soap and water.
- The polarizer is easily damaged and should be handle with special care.Do‘nt press or rub it with hard objects.

☐ PRECAUTION FOR HANDLING LCM

- The LCD module contains a C-MOS LSI.To avoid damage to the LSI from static electricity generated while working,Ground your body,work/assembly areas and assembly equipment to protect the module against STATIC ELECTRICITY.
- Do not input any signal before power is turned on.
- Do not take LCM from it‘s packaging bag until it is assembled.
- Peel off the LCM protective film slowly since static electricity may be generated.
- Pay attention to the humidity of the work shop,50~60%RH is satisfactory.
- Use a non-leak iron for soldering LCM.
- Do not touch the display surface or connection terminals area with bare hands.Smudges on the display surface reduce the insulation between terminals.
- Cautions for soldering to LCM:
  Conditions for soldering I/O terminals:
  Temperature at iron tip: 280°C±10°C.
  Soldering time : 3~4 sec./ terminal.
  Type of solder : Eutectic solder(rosin flux filled).

☐ PRECAUTION FOR STORING LCM

- To avoid degradation of the device,do not store the module under the con itions of direct sunlight,high temperature or high humidity.Keep the module in bags designed to prevent static electricity charging under low temperature / normal humidity conditions(avoid high temperature / high humidity and low temperature below 0 °C).

☐ PRODUCTION NO. DEFINITION