Document Title

256Kx16 bit Low Power full CMOS Static RAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial draft	July 26, 2002	Preliminary
0.1	Revised Added Commercial Product. Deleted 44-TSOP2-400R Package Type.	November 29, 2002	Preliminary
1.0	Finalized - Changed I_{CC} from 10mA to 5mA - Changed $I_{CC}1$ from 10mA to 7mA - Changed $I_{CC}2$ from 50mA to 30mA - Changed I_{SB} from 3mA to 0.4mA - Changed I_{DR}(Commercial) from 15µA to 12µA - Changed I_{DR}(industrial) from 20µA to 12µA - Changed I_{DR}(Automotive) from 30µA to 25µA	September 16, 2003	final

256Kx16 bit Low Power full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 256Kx16
- Power Supply Voltage: 4.5~5.5V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL compatible
- Package Type: 44-TSOP2-400F

GENERAL DESCRIPTION

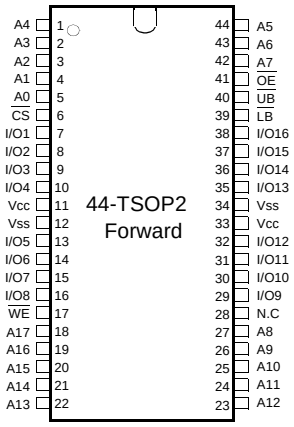
The K6X4016C3F families are fabricated by SAMSUNG′s advanced full CMOS process technology. The families support various operating temperature range and small package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2}, Max)	
K6X4016C3F-B	Commercial(0~70°C)	4.5~5.5V	55[1)]/70ns	20 μA	30 mA	44-TSOP2-400F
K6X4016C3F-F	Industrial (-40~85°C)					
K6X4016C3F-Q	Automotive (-40~125°C)			30 μA		

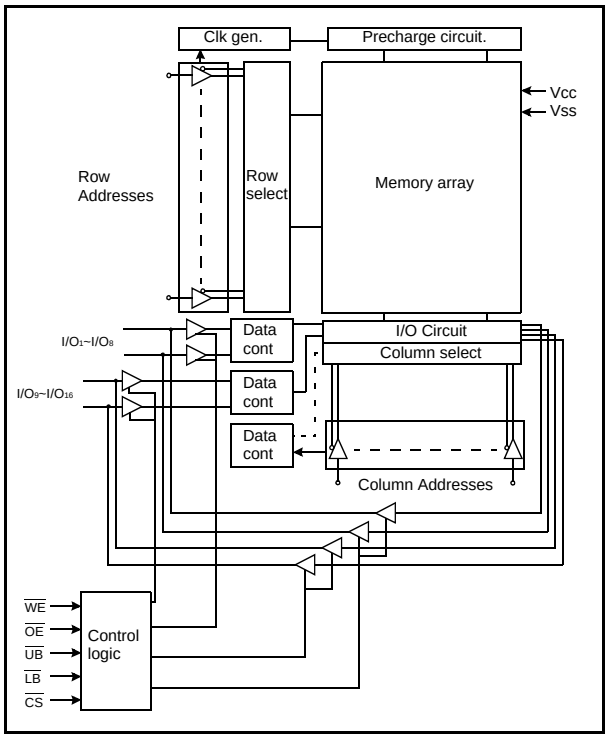
1. The parameter is measured with 50pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS}$	Chip Select Input	$\overline{LB}$	Lower Byte ($I/O_{1\sim8}$)
$\overline{OE}$	Output Enable Input	$\overline{UB}$	Upper Byte($I/O_{9\sim16}$)
$\overline{WE}$	Write Enable Input	Vcc	Power
A_0~A_{17}	Address Inputs	Vss	Ground
I/O_1~I/O_{16}	Data Inputs/Outputs	NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



PRODUCT LIST

Commercial Products(0~70°C)		Industrial Products(-40~85°C)		Automotive Products(-40~125°C)	
Part Name	**Function**	**Part Name**	**Function**	**Part Name**	**Function**
K6X4016C3F-TB55 K6X4016C3F-TB70	44-TSOP2-F, 55ns, LL 44-TSOP2-F, 70ns, LL	K6X4016C3F-TF55 K6X4016C3F-TF70	44-TSOP2-F, 55ns, LL 44-TSOP2-F, 70ns, LL	K6X4016C3F-TQ55 K6X4016C3F-TQ70	44-TSOP2-F, 55ns, L 44-TSOP2-F, 70ns, L

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1~8	I/O9~16	Mode	Power
H	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
L	H	H	X[1]	X[1]	High-Z	High-Z	Output Disabled	Active
L	X[1]	X[1]	H	H	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	Word Read	Active
L	X[1]	L	L	H	Din	High-Z	Lower Byte Write	Active
L	X[1]	L	H	L	High-Z	Din	Upper Byte Write	Active
L	X[1]	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be in low or high state)

ABSOLUTE MAXIMUM RATINGS[1]

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to V_{CC}+0.5V(max. 7.0V)	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.3 to 7.0	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	°C	-
Operating Temperature	T_A	0 to 70	°C	K6X4016C3F-B
		-40 to 85		K6X4016C3F-F
		-40 to 125		K6X4016C3F-Q

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.5[2)]	V
Input low voltage	V_{IL}	-0.5[3)]	-	0.8	V

Note:
1. Commercial Product: T_A=0 to 70°C, otherwise specified
   Industrial Product: T_A=-40 to 85°C, otherwise specified
   Automotive Product T_A=-40 to 125°C, otherwise specified
2. Overshoot: V_{CC}+3.0V in case of pulse width ≤ 30ns
3. Undershoot: -3.0V in case of pulse width ≤ 30ns
4. Overshoot and undershoot are sampled, not 100% tested

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested

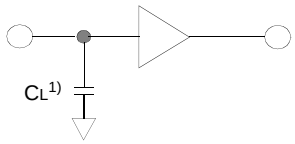
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	µA
Operating power supply current	I_{CC}	I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, Read		-	-	5	mA
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA $\overline{CS}$≤0.2V, V_{IN}≥0.2V or V_{IN}≥Vcc-0.2V		-	-	7	mA
	I_{CC2}	Cycle time=Min, 100% duty, I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}		-	-	30	mA
Output low voltage	V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)	I_{SB}	$\overline{CS}$=V_{IH}, Other inputs = V_{IL} or V_{IH}		-	-	0.4	mA
Standby Current(CMOS)	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, Other inputs=0~Vcc	K6X4016C3F-B	-	-	20	µA
			K6X4016C3F-F	-	-		
			K6X4016C3F-Q	-	-	30	µA

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.8 to 2.4V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load (See right): C_L=100pF+1TTL
C_L=50pF+1TTL



1. Including scope and jig capacitance

AC CHARACTERISTICS

(Vcc=4.5~5.5V, Commercial Product: T_A=0 to 70°C, Industrial Product: T_A=-40 to 85°C, Automotive Product : T_A=-40 to 125°C,)

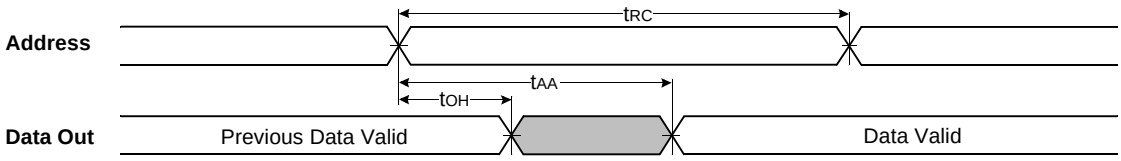
Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t_{RC}	55	-	70	-	ns
	Address access time	t_{AA}	-	55	-	70	ns
	Chip select to output	t_{CO}	-	55	-	70	ns
	Output enable to valid output	t_{OE}	-	25	-	35	ns
	Chip select to low-Z output	t_{LZ}	10	-	10	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	5	-	ns
	$\overline{LB}$, $\overline{UB}$ enable to low-Z output	t_{BLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t_{HZ}	0	20	0	25	ns
	$\overline{OE}$ disable to high-Z output	t_{OHZ}	0	20	0	25	ns
	Output hold from address change	t_{OH}	10	-	10	-	ns
	$\overline{LB}$, $\overline{UB}$ valid to data output	t_{BA}	-	25	-	35	ns
	$\overline{UB}$, $\overline{LB}$ disable to high-Z output	t_{BHZ}	0	20	0	25	ns
Write	Write cycle time	t_{WC}	55	-	70	-	ns
	Chip select to end of write	t_{CW}	45	-	60	-	ns
	Address set-up time	t_{AS}	0	-	0	-	ns
	Address valid to end of write	t_{AW}	45	-	60	-	ns
	Write pulse width	t_{WP}	45	-	55	-	ns
	Write recovery time	t_{WR}	0	-	0	-	ns
	Write to output high-Z	t_{WHZ}	0	20	0	25	ns
	Data to write time overlap	t_{DW}	25	-	30	-	ns
	Data hold from write time	t_{DH}	0	-	0	-	ns
	End write to output low-Z	t_{OW}	5	-	5	-	ns
	$\overline{LB}$, $\overline{UB}$ valid to end of write	t_{BW}	45	-	60	-	ns

DATA RETENTION CHARACTERISTICS

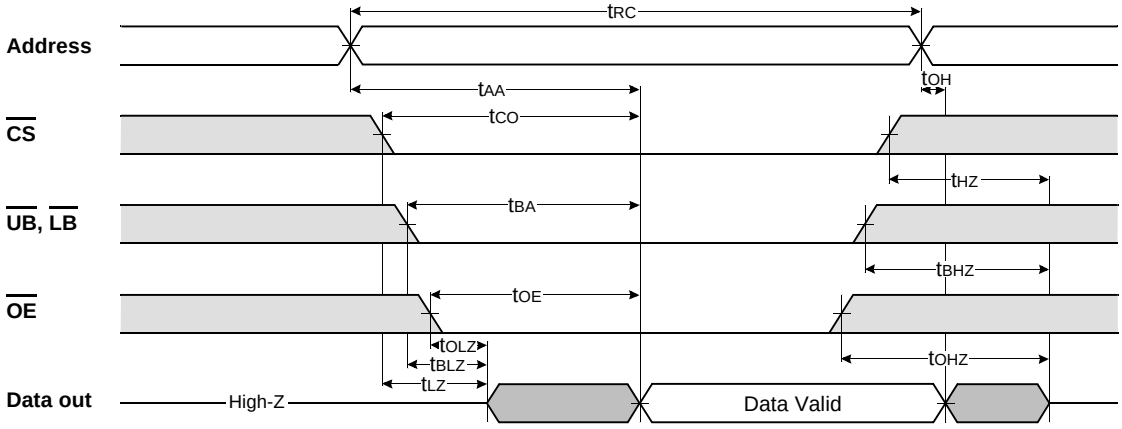
Item	Symbol	Test Condition		Min	Typ	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS}$≥Vcc-0.2V		2.0	-	5.5	V
Data retention current	I_{DR}	Vcc=3.0V, $\overline{CS}$≥Vcc-0.2V	K6X4016C3F-B		-	12	µA
			K6X4016C3F-F			12	
			K6X4016C3F-Q			25	
Data retention set-up time	t_{SDR}	See data retention waveform		0	-	-	ms
Recovery time	t_{RDR}			5	-	-	

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})



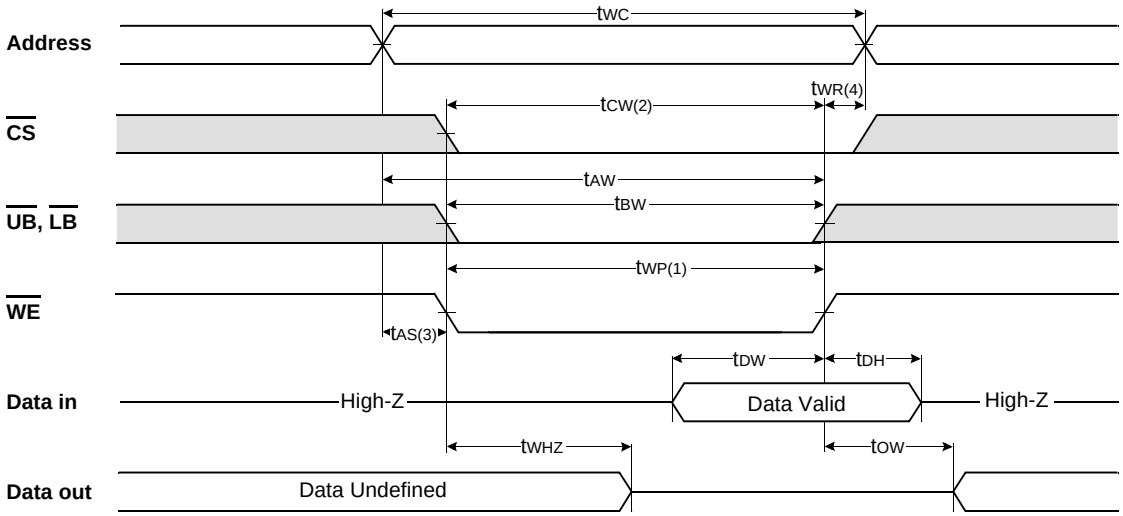
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



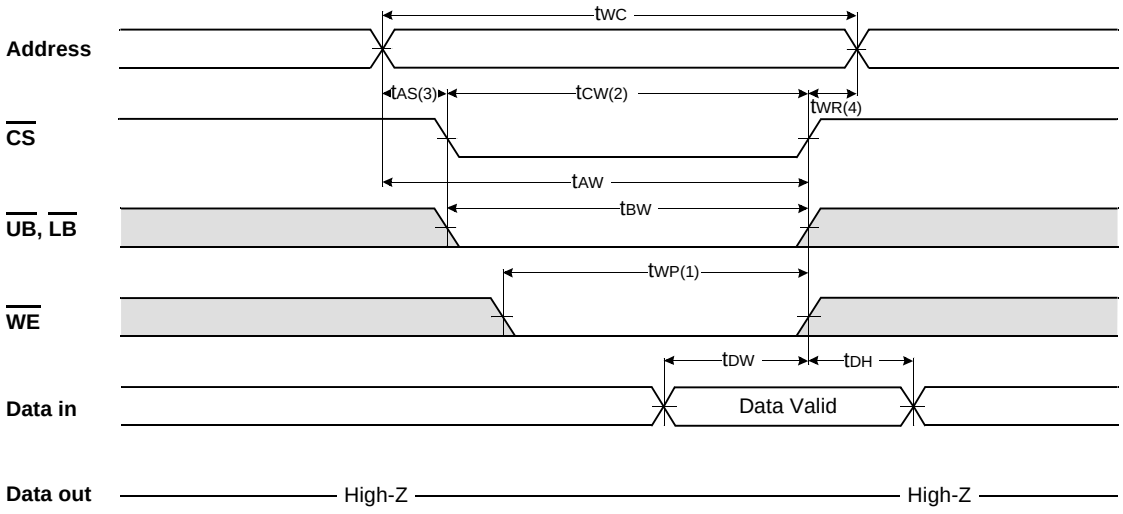
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

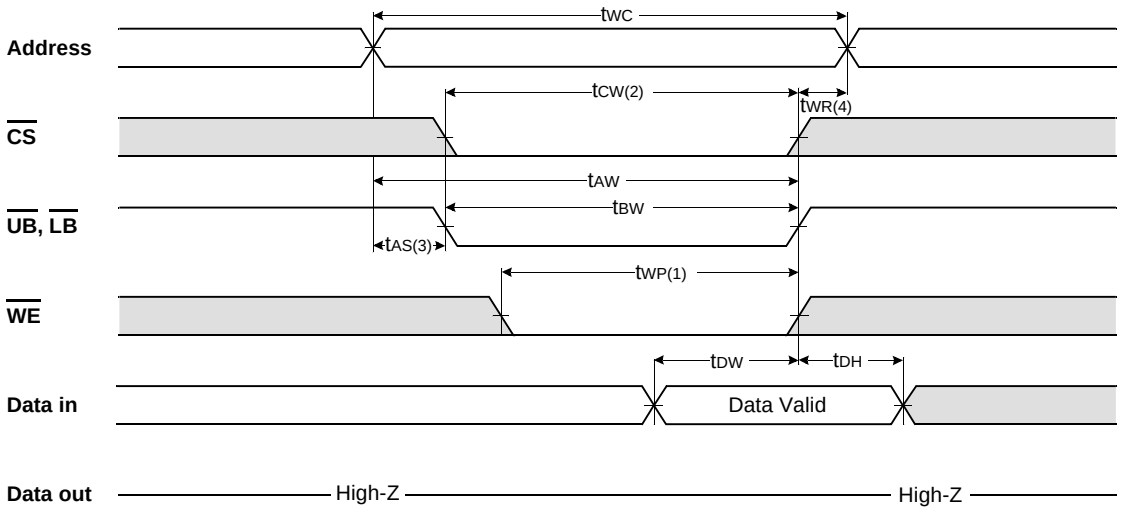
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)

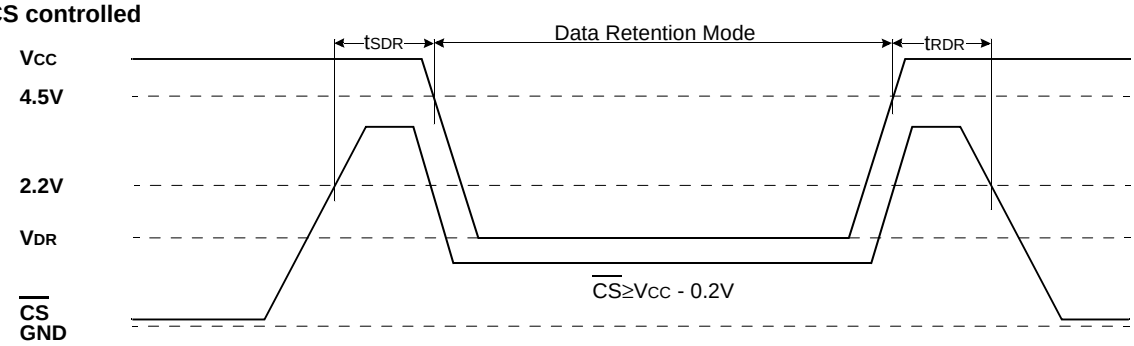


NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

$\overline{CS}$ controlled



PACKAGE DIMENSIONS

Units: millimeter(inch)

44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)