

## How to Minimize Power Dissipation in Li+ Linear Chargers

Techniques are described for minimizing power dissipation in linear battery chargers. Beginning with a stable wall-cube switching power source, methods are described to limit the dissipation in the linear charging circuit. Circuits are provided, calculations are shown, heat sinking for the PMOS pass transistor is discussed, and suitable pass transistors are suggested.

### Introduction

Data sheets for single-cell Li+ linear chargers seldom discuss power dissipation or how to deal with heat dissipation. High input voltage and charge current increase the amount of power the pass element must handle. This application note discusses how to maximize charging current while maintaining safe device and system temperature limits.

### Use a Proper DC Input Source

A low voltage input reduces the power dissipation. In order to charge the single-cell Li+ battery, we need a well regulated 4.2V±1% or 4.1V±1% (depending on battery chemistry) output. The input voltage needs to be higher to cover the voltage drops between the battery positive terminal and the input DC source. Figure 1 shows these for a typical charger.

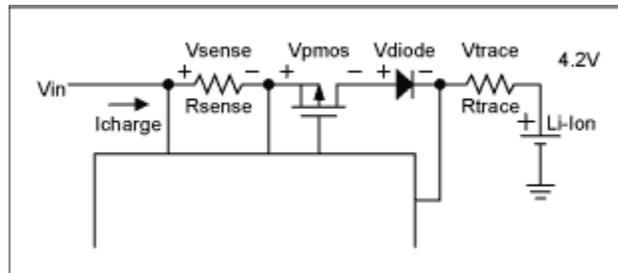


Figure 1. Voltage drop contribution

$$V_{in} = V_{sense} + V_{pmos} + V_{trace} + V_{diode} + 4.2V$$

The minimum input can be described as below.

$$V_{in(min)} = R_{sense} \cdot I_{charge} + R_{ds(on)} \cdot I_{charge} + R_{trace} \cdot I_{charge} + (V_{thmax(d)} + R_d \cdot I_{charge}) + 4.2V$$

Where  $V_{diode} = V_{thmax(d)} + R_d \cdot I_{charge}$ ,  $V_{thmax(d)}$ ; Diode turn on threshold voltage,  $R_d$ ; Diode series resistance

As we see in the above equation, the charger requires higher input voltage if the charge current ( $I_{charge}$ ) is increased. Below is actual data from an example circuit (Figure 4) when the charge current is 500mA.

$$V_{in} = 0.303V(V_{diode}) + 0.060V(V_{sense}) + 0.112V(V_{pmos}) + 0.000V(V_{trace}) + 4.2V$$

$$V_{in} = 4.68V$$

Schottky diode: Zetex ZHCS1000,

PMOS FET: Fairchild FDC636P,

$$R_{sense} = 105m\Omega,$$

Rtrace: 40mils wide, 0.5" long, and 1 oz copper trace. This value depends upon PCB layout and battery contacts.

Since this data was taken from one prototype, we should also consider the tolerances of each parameter. A  $5V \pm 5\%$  well-regulated switching mode AC adapter will provide some margin, to account for tolerances. The AC adapter does not need an accurate current limit since the charger has a current control, but the AC adapter maximum current capability must be 200-300mA higher than the fast charge current of the linear charger. Figure 2 shows an example of an AC adapter using a MAX5021 low-power, current-mode PWM controller.

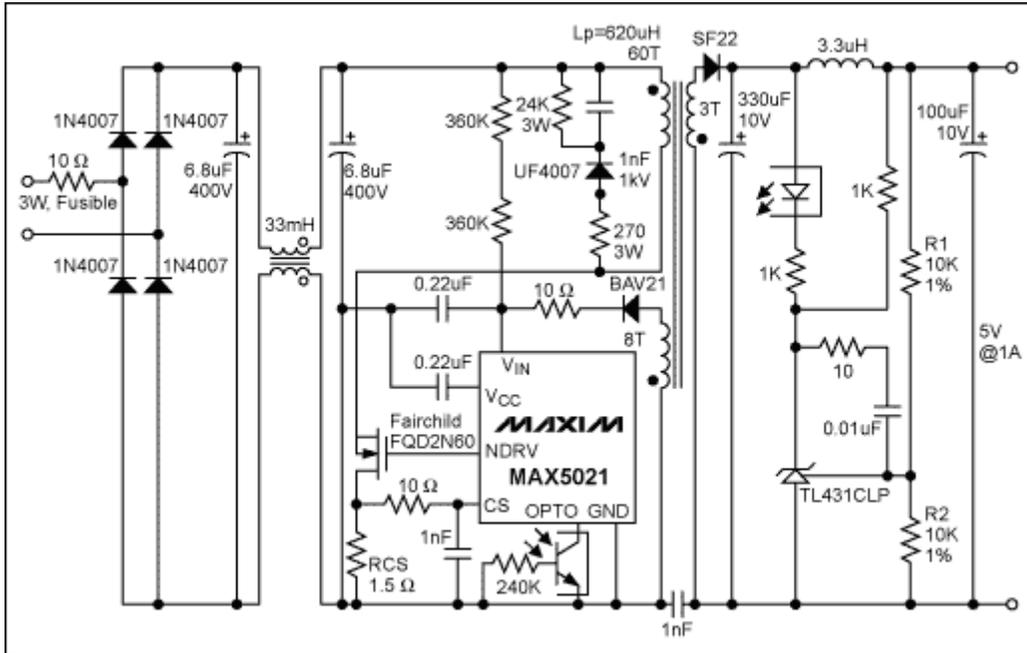


Figure 2. 5V/1A AC adapter

## Optimize Charge Current and Power Dissipation

Figure 3 shows the circuit used for testing. It is a linear charger with a 500mA charge current and a 6 hours timer limit.

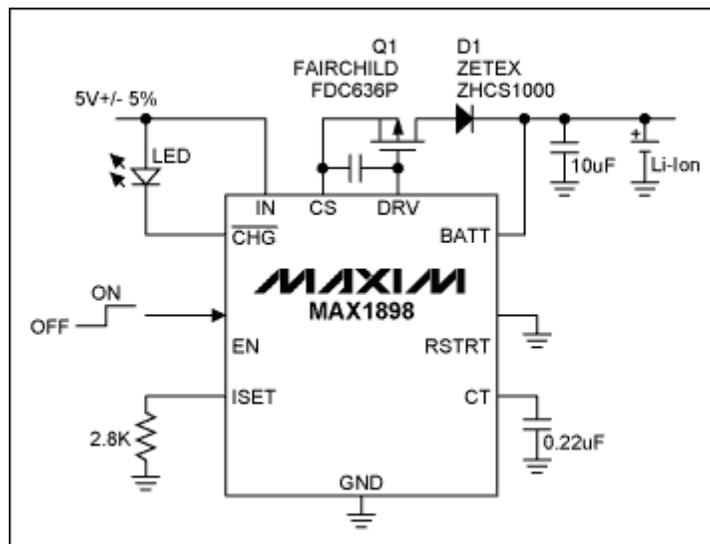


Figure 3. The MAX1898 single-cell Li+ linear charger

Total power dissipation for the linear charger can be expressed as below.

$$P_{diss} = (V_{in} - V_{batt}) \cdot I_{charge}$$

To decide the fast charging current, we need to calculate the worst-case allowable power dissipation on the P-MOSFET Q1.

Power dissipation on the Q1 is expressed as below:

$$P_{diss}(Q1) = V_{ds}(Q1) \cdot I_{charge}$$

$$V_{ds}(Q1) = 5V - V_{D1} - I_{charge} \cdot R_{cs} - V_{batt}$$

Where  $V_{D1}$ : D1 forward voltage drop,  $R_{cs}$ : internal current sensing resistor.

Also, the junction temperature of the P-MOSFET should not exceed its maximum limit = 150°C at any operating conditions.

$$T_j = T_a + R_{\theta JA} \cdot P_{diss}(Q1)$$

Table 1 shows some possible P-MOSFET products that can be used in the charger. Even though the specifications show quite high maximum power dissipations, we should be cautious of the PCB mount condition. The "1 in\_ pad of 2oz Cu on FR-4 board" specified for package rating on many MOSFET devices may not be realistic for many applications. Instead, the following design procedure yields more practical results

**Table 1**

	Package	Pd, Maximum Power Dissipation	$R_{\theta JA}$ , $R_{\theta JC}$ , $R_{\theta CA}$ Thermal Resistance	PCB Mount
FAIRCHILD FDC636P	SuperSot-6	1.6W at 25°C	$R_{\theta JA}$ = 78°C/W $R_{\theta JC}$ = 30°C/W $R_{\theta CA}$ = 48°C/W	1 in_ pad of 2oz Cu on FR-4 board.
		0.8W at 25°C 0.417W at 85°C	$R_{\theta JA}$ =156°C/W $R_{\theta JC}$ = 30°C/W $R_{\theta CA}$ = 26°C/W	Minimum pad of 2oz Cu on FR-4 board.
Vishay Siliconix Si3441DV	TSOT-6	1.1W at 25°C	$R_{\theta JA}$ =110°C/W $R_{\theta JC}$ = 30°C/W $R_{\theta CA}$ = 80°C/W	Surface Mounted on 1 in_ FR4 board
		0.6W at 85°C		
Vishay Siliconix Si5443DC	1206-8 ChipFET	1.3W at 25°C	$R_{\theta JA}$ =95°C/W $R_{\theta JC}$ = 20°C/W $R_{\theta CA}$ = 75°C/W	Mounted on 1 in_ FR4 board

At first, we should figure out the best  $R_{\theta JA}$  that we could get given the system design restrictions. The  $R_{\theta JA}$  is the sum of the junction-to-case ( $R_{\theta JC}$ ) and case-to-ambient thermal resistance ( $R_{\theta CA}$ ), where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta CA}$  is determined by the user's board design, heatsinking method, and a cooling system. We should reduce the  $R_{\theta CA}$  as low as possible. However, there will be some restrictions such as a limited board space, no ventilation, and safety requirements for PCB material. Since we cannot measure the  $T_j$  directly, we can use  $T_c$  to compute  $R_{\theta CA}$ .

$$T_c = T_a + R_{\theta CA} \cdot P_{diss}(Q1)$$

$$R_{\theta CA} = (T_c - T_a) / P_{diss}(Q1)$$

To design an efficient heatsink for a surface mount PMOS FET, we should increase the drain pin board areas as much as we can. And then we can measure the  $V_{d-s}$  (Q1),  $I_{charge}$ , and  $T_c$  to calculate  $R_{\theta CA}$ . If the measured  $R_{\theta CA}$  is lower than what we expect, we should increase the surface area of the drain pin pads or reduce the charge current. Also, we should keep in mind that  $T_c$  must not exceed 130°C or 150°C PCB maximum operating temperature, depending upon PCB materials. We should check UL file numbers of PCB material that we use and their maximum operating temperature before we start. Let's assume we are using FR-4 two layer boards rated at 130°C max.

If the measured case temperature  $T_c$  is 125°C at  $T_a = 50^\circ\text{C}$  and  $P_{diss}(Q1) = 800\text{mW}$ ,

$$125^\circ\text{C} = 50^\circ\text{C} + R_{\theta CA} \times 800\text{mW}$$

$$R_{\theta CA} = (125^\circ\text{C} - 50^\circ\text{C}) / 0.8\text{W}$$

$$= 93.75^\circ\text{C/W}$$

If  $R_{\theta CA} = 93.75^\circ\text{C/W}$ ,  $R_{\theta CJ} = 30^\circ\text{C/W}$  (TSOP-6),  $T_a(\text{max}) = 50^\circ\text{C}$ , and  $T_j(\text{max}) = 150^\circ\text{C}$ , the maximum power dissipation that we can achieve;

$$150^\circ\text{C} = 50^\circ\text{C} + 123.75^\circ\text{C/W} \cdot P_{diss}(Q1)$$

$$P_{diss}(Q1)_{\text{max}} = 808\text{mW}$$

If the initial  $V_{batt} = 3.0\text{V}$ ,  $R_{cs} = 105\text{m}\Omega$ , and  $V_{D1} = 0.35\text{V}$  at  $I_{charge} = 500\text{mA}$ , the worst case  $V_{ds}(Q1)_{\text{max}}$  is;

$$V_{ds}(Q1)_{\text{max}} = 5\text{V} - V_{D1} - I_{charge} \cdot R_{cs} - V_{batt} = 1.40\text{V}$$

The allowable maximum charge current is:

$$I_{charge}(\text{max}) = P_{diss}(Q1)_{\text{max}} / V_{ds}(Q1)_{\text{max}}$$

$$= 808\text{mW} / 1.60\text{V}$$

$$= 505\text{mA}$$

Of course, the power dissipation will gradually drop as the battery voltage rises.

## Conclusion

We can deliver a safe and reliable linear charger for a single-cell Li+ battery by optimizing the DC input source, the charge current, and the power dissipation with proper heatsinking method. Figure 4 shows an actual test result using the MAX1898 charger with a 4.2V, 900mA Li+ cell and a regulated 5V/1A MAX5021 AC adapter.

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### MORE INFORMATION

MAX1898: [QuickView](#)

-- [Full \(PDF\) Data Sheet \(224k\)](#)

-- [Free Sample](#)

MAX5021: [QuickView](#)

-- [Full \(PDF\) Data Sheet \(256k\)](#)

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